Modeling of Integrated RF Passive Devices

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Abstract—We describe the use of an electromagnetic (EM) simulator for modeling integrated RF components and circuits. Modern EM simulators are fast and accurate enough to provide good models of such components. An important aspect of advanced IC processes is that the physical properties of wires (width, thickness, and resistance) vary depending on the surrounding wiring. We discuss how the EMX simulator [1] handles width and spacing-dependent properties in the process description. Because the simulator handles mask-ready layout without the need for manual simplification, it is feasible to simulate thousands of possible designs and build scalable component models. Such scalable models allow fast choices of optimal components that meet user-supplied specifications.

I. INTRODUCTION

Technology trends have made on-chip passive components pervasive. Thick metals and high-resistivity substrates lead to high-quality on-chip inductors, transformers, and baluns. For example, integrated baluns can now be designed that have insertion loss comparable to off-chip LTCC or ceramic baluns. High-density interdigitated (MoM) capacitors are possible because of fine feature sizes (0.1 µm and below) and a large number of interconnect layers (ten or more). IC processes also offer tight tolerances, so variability from chip to chip is low. And of course integration offers cost savings as well. Because of their increased prevalence, fast and accurate modeling of integrated passives is important. There are two main aspects of this modeling:

1) EM simulation to evaluate candidate physical designs, and possibly to refine the physical design.

2) Converting the EM simulation results into models that can be used with higher level simulators, e.g., at the circuit netlist level.

EM simulators fall into two broad categories: those based on a differential formulation of Maxwell’s equations, and those based on integral formulations. Examples of the former include finite difference (both frequency- and time-domain) and finite element simulators [2]. These offer flexibility, but have the drawback that dielectrics, including a suitably large amount of space surrounding the physical conductors, must be discretized. This is because Maxwell’s equations must be enforced wherever there is a non-trivial field. Integral (or boundary element) formulations [3] are typically frequency-domain, and are most appropriate when the enclosing dielectric media is largely planar. They require discretization only of the conductors, not the surrounding dielectrics. For IC passives, planarity is an excellent approximation. Further, understanding of how to efficiently implement boundary-element methods has increased notably with the development of the Fast Multipole Method and related techniques [4]. Overall, frequency-domain integral methods are usually the most efficient choice when they are applicable, and hence are the most appropriate for simulation of IC passives. We will concentrate on these methods.

Converting frequency-domain simulation data into a form suitable for a circuit simulator is a difficult problem in the general case. However, in the more constrained domain of modeling basic types of components, there are two basic approaches. One is to use an optimizer to pick the parameters of a user-specified circuit topology that is appropriate to the device. While non-linear optimization in general is difficult, it works reasonably well for this application. Approaches based on pole-zero fitting are also workable. Care must be taken to maintain passivity, but commercial tools are available, both internally in some circuit simulators [5] or as stand-alone applications [6]. Either optimization or pole-zero fitting are appropriate for modeling individual passive components. Optimization also offers the possibility of making scalable models. A scalable model is parameterized by physical quantities. For example, a scalable inductor model might be parameterized by number of turns, diameter, wire width, and turn-to-turn spacing. A scalable model captures the whole design space of possible components. Having a scalable model makes it possible to quickly synthesize an optimal design from a user-supplied specification by searching the entire design space [7].

II. INTEGRAL FORMULATIONS FOR EM SIMULATION

Planar EM simulators based on integral formulations only require discretization of the conductors, not the surrounding dielectrics. All of the dielectric and substrate effects are implicitly captured in the form of a Green’s function [8]. In the frequency domain, the stimulus electric field $E_s$ at a point $r$ must match the field arising from ohmic losses, the vector potential $A$ and the scalar potential $\phi$:

$$E_s(r) = \frac{1}{\sigma} J(r) + j \omega A(r) + \nabla \phi(r).$$ (1)

The vector and scalar potentials are obtained by integrating over the conductors: $A(r) = \int G_A(r,r') J(r') dr'$, and $\phi(r) = \int G_\phi(r,r') \rho(r') dr'$. $J$ is the current density, $\rho$ is the charge density, $G_A$ is the vector potential Green’s function, and $G_\phi$ is the scalar potential Green’s function. For computer simulation, this continuous equation is discretized by cutting the conductors up into individual mesh elements, each with an
unknown charge and/or current. The integrals become finite sums, and the problem can be expressed as a linear system.

Because of the integrals over conductor surfaces, integral formulations give rise to dense systems of linear equations after discretization. That is, a bit of current or charge in one mesh element influences the potentials in all of the other mesh elements. Dealing with this dense system of equations made early simulators that used integral formulations comparable in speed to those that used differential formulations, despite the fact that the former required only a small number of discretization elements. Later research in iterative methods for the solution of linear systems [9] and in techniques for compactly representing the linear systems that arise from integrals involving potentials [4] dramatically increased the speed of integral formulation simulators. The techniques pioneered in first generation fast field solvers from research institutions [10], [11], [12], [13], [14] have been making their way into commercial tools such as Agilent’s Momentum [15], Ansoft’s Q3D Extractor [16], and Integrand Software’s EMX [1]. These tools have added further improvements in speed and memory efficiency. Additional refinements such as the use of fast direct solvers are now appearing in academic contexts [17]. Since we are familiar with the internals of EMX, we will discuss some of the refinements that it uses [18].

In order to accurately model IC layouts, it is important to simulate skin-effect and sidewall capacitances correctly. Especially for MoM capacitors, a “2.5D” approximation using thin conductors is insufficient. We use a volume integral formulation that treats conductors and vias as true 3D objects, as shown in figure 1.

EMX uses a special representation of the vector potential interactions (normally the most computationally expensive part of the simulation). The representation allows the vector potential interactions to be computed with about the same cost as the scalar interactions. The method depends on decomposing the currents into divergence-free and curl-free parts. The divergence-free parts give the dominant contributions to the vector potential, and these are captured exactly. The less-important contributions of the curl-free part are approximated in a way that is accurate to a bit better than 1%, which suffices for IC problems.

Typical IC layouts are very regular. Beyond repeated instances of a subcircuit or component, wires tend to be paths of constant width, the distance between adjacent routing is typically constant, and most routing is at 90 or 45 degree angles. Simulators can use regularity to reduce both time and memory requirements. Figure 2 shows repeated shapes in the mesh of an inductor that can be exploited.

In practice, automation is just as important as simulation speed and memory efficiency. If getting the layout into a suitable form for the simulator requires significant hand editing, the human becomes the bottleneck. Most commercial EM simulators have interfaces to the major IC design systems, and they have methods for automating tasks such as via merging. EMX automatically handles features typical of modern IC layouts, such as via arrays, context-dependent contacts, and metal fill and slotting.

III. PATTERN-DEPENDENT EFFECTS

One feature of advanced IC processes is that the physical width, thickness, and resistance of a wire generally depends on the surrounding wiring. Sometimes the variations are very significant. Fabricated widths may vary by up to 50% from the nominal (drawn) width, and sheet resistance can change by a factor of two. Such variations are called pattern-dependent effects. Because these effects can be so large, it is important to account for them in simulation and modeling.

Some foundries now provide detailed information about pattern dependencies. This information is usually in the form of tabulated data, with the tables indexed by wire width and spacing to adjacent wires. An example is TSMC’s interoperable R(L)C extraction technology file format iRCX [19], [20]. This file format is now used for both static RLC extraction and high frequency EM simulations.

The process description used by a simulator must include all of the definitions of material properties (such as dielectrics and conductivities) and all the cross-section dimensions (layer and conductor thicknesses). EMX also allows the specification of conductor properties to include width and spacing dependencies. Internally, the the input (drawn) layout is automatically modified in order to accurately model the fabricated structure. Handling pattern-dependent effects requires:

- devising appropriate definitions of the local width and spacing and developing efficient algorithms for computing these quantities; and
- manipulating the input geometry as a function of them.

We discuss these steps in the following two subsections.
A. Computing Width and Spacing

For simple repetitive layout (e.g., multiple parallel wires) width and spacing have intuitive meanings. However, a simulator must handle more complicated situations involving non-uniform layout. We want definitions that match the intuitive meanings in regular regions and that lend themselves to efficient computation. For width and spacing, a natural geometric data structure for representing local distances between objects is the Voronoi diagram [21].

In the case of layout, the objects of interest are line segments representing the edges of wires, and points where segments join. Each segment and point has a region around it that is closer to that object than to any other object. Following this idea, the entire plane is partitioned into non-overlapping regions, and this partitioning is the Voronoi diagram of the segments and points. Note that part of the Voronoi diagram lies within the wiring, and the rest lies outside. These two parts are called the interior and exterior Voronoi diagrams. A portion of a MoM capacitor layout and the associated exterior Voronoi diagram is shown in figure 3. The shaded areas are the wires. Between the wires, there are some segments which represent the boundaries of the Voronoi regions. Also shown are some maximal inscribed circles. Each such circle just touches three objects, and the circles cannot be made any bigger while touching those objects.

The local spacing is taken from the diameter of the appropriate maximal inscribed circle that touches the segment and the nearest other object(s). The local width is calculated in the same way as the local spacing, except it is based on the interior Voronoi diagram instead of the exterior one. Local width and spacing can be calculated at key points throughout the layout during the Voronoi diagram construction. Afterwards, the values can be quickly interpolated at any desired location.

B. Mimicing Fabrication Effects

Typically the most significant fabrication effect is that physical line width differs from the drawn width by a bias amount which depends on the local width and spacing in the layout. The bias is obtained from a table provided by the foundry. Table I shows an example of how the physical width of a metal wire depends on the drawn width and spacing. For example, a 0.1 \( \mu \)m drawn wire at a spacing of 0.2 \( \mu \)m will physically expand to be 0.147 \( \mu \)m wide. That represents an increase of almost 50% from the drawn width.

Interpolating in such a table produces a continuous function for the bias as a function of drawn width and spacing. An example of a layout before and after such a variable bias operation is shown in figure 4. Note that the biased geometry is not rectilinear when the width and spacing are not uniform.

Another significant effect is sheet resistance variation. After calculating the local width and spacing and the biased geometry, the simulator can proceed with mesh generation as normal. Then at each point in the mesh, the sheet resistance can be calculated as a function of width and spacing. Each shape in the mesh may be assigned a sheet resistance by averaging over the area of the shape. An example of how resistance varies is shown in table II. Note that the sheet resistance changes by almost a factor of two as a function of width and spacing. Figure 5 shows the variation in sheet resistance for a MoM capacitor.

IV. Examples

We start with three examples that show the size of problems that can be handled by a modern EM simulator. The ability to simulate larger blocks containing multiple components allows modeling more complicated structures where interactions between components are also taken into account. All these examples were run using EMX on a machine with eight

| \( w \times s \) | 0.1000 | 0.1025 | 0.1125 | 0.1220 | 0.1470 | . . . |
| 0.1000 | 0.1265 | 0.1285 | 0.1340 | 0.1525 | . . . |
| 0.1300 | 0.1459 | 0.1459 | 0.1459 | 0.1599 | . . . |
| 0.1500 | 0.1783 | 0.1783 | 0.1783 | 0.1783 | . . . |
| 0.2000 | . . . | . . . | . . . | . . . | . . . | . . . |

Table I

Example variation of physical width (microns) as a function of drawn width and spacing.
TABLE II
EXAMPLE VARIATION OF SHEET RESISTANCE (OHMS/SQUARE) AS A FUNCTION OF DRAWN WIDTH AND SPACING

<table>
<thead>
<tr>
<th>w (μm)</th>
<th>0.1000</th>
<th>0.1300</th>
<th>0.1500</th>
<th>0.2000</th>
<th>. . .</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1000</td>
<td>0.1399</td>
<td>0.1230</td>
<td>0.1084</td>
<td>0.0839</td>
<td>. . .</td>
</tr>
<tr>
<td>0.1300</td>
<td>0.1355</td>
<td>0.1316</td>
<td>0.1255</td>
<td>0.1034</td>
<td>. . .</td>
</tr>
<tr>
<td>0.1500</td>
<td>0.1285</td>
<td>0.1275</td>
<td>0.1266</td>
<td>0.1116</td>
<td>. . .</td>
</tr>
<tr>
<td>0.2000</td>
<td>0.1315</td>
<td>0.1305</td>
<td>0.1295</td>
<td>0.1286</td>
<td>. . .</td>
</tr>
<tr>
<td>. . .</td>
<td>. . .</td>
<td>. . .</td>
<td>. . .</td>
<td>. . .</td>
<td>. . .</td>
</tr>
</tbody>
</table>

Fig. 5. Variation of sheet resistance in the mesh

2.5 GHz CPUs and 24 GB of memory. The speed-up for eight CPUs compared to a single CPU depends on the characteristics of the example and the number of ports, but it can be up to six. In all of the examples, the input was mask-ready GDSII layout. No hand-editing or simplification was done for any of the examples. Wall-clock simulation times for even the largest example was under two hours, fast enough that EM simulation can be part of the design process instead of being used only as a final step during “sign-off.” The maximum memory requirement was under 10 GB.

A. IC Diplexer

Figure 6 shows an integrated diplexer in a 0.18 μm 5-layer metal BiCMOS technology. The design contains resistors, inductors, MiM capacitors, and probe pads. One main issue for the designers was accounting for all of the couplings between inductors, and between inductors and interconnect. Direct simulation of the whole structure ensured that no significant interactions were missed. Comparisons of the high-and low-band simulated and measured responses (figure 7) show excellent agreement.

B. VCO

Figure 8 is an integrated VCO fabricated in a 6-layer 90 nm CMOS technology. It consists of an inductor and a bank of 66 MiM capacitors that are switchable for tuning. The inductor here is small, enough so that parasitic coupling between the inductor and the interconnect and the details of how the capacitors are hooked up must be considered. Indeed, a block-by-block model failed to predict the VCO’s behavior. Simulating the whole structure gave much more accurate results. The simulated and measured tuning curves are shown in figure 9.

C. IPD Diplexer

Figure 10 shows another diplexer built in an IPD (Integrated Passive Device) technology. The design includes resistors, inductors, and thin-film capacitors, plus the measurement pads.
EM simulation was an integral part of this design. Starting from the diplexer specification, an appropriate topology and approximate component values were chosen. A preliminary layout included the coils and ports where tuning capacitors should connect, but the capacitor values were not yet fixed. EM simulation produced a model that was used in a circuit simulator and optimizer to pick appropriate capacitor values. A final EM simulation confirmed that the device should meet specifications, just as subsequent measurements proved. Figure 11 compares simulations and measurements for the IPD diplexer.

D. Pattern-Dependent Effects

Here we show the significance of pattern-dependent effects by comparing simulations and measurements for MoM capacitors and stacked inductors. The technology is TSMC’s 65 nm 9-metal process, and the width and spacing dependencies are given by an iRCX file.

The MoM capacitors vary in the number of metals used, the widths of the metal fingers, and the spacings between fingers. For this 65 nm technology the minimum width and minimum spacing are both 0.1 µm. A mesh of one of the MoM capacitors is shown in figure 12.

We did two sets of simulations: once with the wire properties fixed at their minimum-width, minimum-spacing values (no iRCX), and once with the full iRCX information that allowed EMX to mimic the fabricated layout. Figure 13 shows the measured and simulated (low frequency) capacitance values for these MoM capacitors. For capacitors with minimum width and minimum spacing, both simulations provided excellent agreement with measurements. However, for MOM36 with width 0.1 µm and spacing 0.16 µm there is a 0.2% error when the iRCX file is used and a 13% error when it is not. This ties in with the iRCX table in table I, which shows that the bias is most significant for wires that have increased width or spacing.

Figures 13 and 14 show the high-frequency characteristics of the capacitors. For MOM06, with minimum width and spacing, both iRCX and non-iRCX simulations agree well with

<table>
<thead>
<tr>
<th>cell</th>
<th>meas w, s µm</th>
<th>iRCX</th>
<th>no iRCX</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOM06</td>
<td>0.1, 0.1</td>
<td>0.611</td>
<td>0.617</td>
</tr>
<tr>
<td>MOM67</td>
<td>0.16, 0.16</td>
<td>0.293</td>
<td>0.295</td>
</tr>
<tr>
<td>MOM27</td>
<td>0.1, 0.16</td>
<td>0.061</td>
<td>0.061</td>
</tr>
<tr>
<td>MOM36</td>
<td>0.1, 0.16</td>
<td>0.682</td>
<td>0.680</td>
</tr>
</tbody>
</table>
measurements. However, for MOM36 the iRCX simulation has excellent agreement while the and non-iRCX simulations has a large discrepancy in C and Q.

We also simulated a stacked inductor. The inductor winds from metal 5 through metal 9, and includes two thin metals as well as the two thicker ones. The Q of the inductor depends significantly on the resistance in the thin metals, and this resistance varies as a function of metal width and the spacing to nearby wires. This is exactly the effect seen in measurement (figure 15). Again, the simulation taking width and spacing dependence into account is significantly more accurate.

**E. Balun Modeling and Synthesis**

Now we discuss the production of a scalable model that is suitable for synthesis of optimal components. As an example, we consider on-chip baluns.

We start with a transformer layout generator whose inputs are turns ratio, number of turns, trace width and coil diameter. In the first step, we used EM simulator to characterize the range of about 1000 possible transformer layouts. Thanks to the simulators efficiency and automated layout handling, it required only a day to cover the full possible design space: wire width of 4 to 10µm, 2 through 5 turns, a turns ratio of 1:1 through 1:4, and a diameter of 50 to 400µm.

In the next step, we use optimization to create an accurate scalable model parameterized by these same physical design parameters. The topology for the scalable model was derived from physical intuition and is shown in Figure 16. The schematic shows a center-tapped pair of coils. Each coil includes additional resistors and inductors for modeling skin-effect. A combination of resistors and capacitors is used to model the substrate.

Each element in the model has a value that is a non-linear function of the geometric parameters. The specific forms of these functions are chosen based on physical intuition. For example, the main series resistance in each coil is proportional to the diameter and inversely proportional to the width. The fitting coefficients within the functions are determined by a non-linear least squares optimizer. A playback was done of the model compared to the individual EM simulations, and the model was verified to match within a few percent for derived quantities like inductance, $k$, Q, etc. For example, the histogram of Figure 17 shows the percentage error in primary inductance $L_1$, secondary inductance $L_2$, and $k$ across the design space. The optimizer took a few hours to build the scalable model.

Given the scalable model of the transformer, simulation
of the performance of any particular balun (including the tuning capacitors) takes only a fraction of a second. This means that an exhaustive examination of the entire design space can be done in under a minute. Constraints may be placed on any combination of area, insertion loss, return loss (matching), phase imbalance or amplitude imbalance. The entire bandwidth of interest can be checked, and the desired input and output impedances can also be specified during the search. While the EM simulation and the construction of the scalable model is time-consuming, the actual synthesis of any given balun is very quick. Such scalable models derived from EM simulations and linked with optimal synthesis capabilities are now provided by some foundries as part of their design kits for components like inductors, capacitors, transformers, and baluns.

This method was used to design four baluns for common applications: 802.11A, 802.11B, DCS and GSM. A standard single-ended impedance of 50Ω and a differential output impedance of 200Ω were chosen for demonstration. The baluns were fabricated in UMC’s 90nm, 9-level IC process. 3µm copper was used for the coil, and thinner metals were stacked to form the underpasses. Tuning MIM capacitors of 2fF/µm² were used. In all the layouts, coil area dominated capacitor area. A chip photograph of one of the fabricated baluns is shown in figure 18.

Two sets of layouts were fabricated for verification. The first set had the four transformers with center-tap floating in a four port pad frame. The second set was the baluns, i.e., the same transformers along with the tuning capacitors (and the center tap grounded). Figure 19 shows the comparison of measurement to the direct EM simulation of the DCS transformer. The agreement is excellent and inductance and k value are within a few percent of measurements across the entire frequency band.

The results were equally good for the other three transformers and are summarized in Table IV, showing the inductance and coupling values at 1GHz.

Figure 20 shows the comparison of measurement to the direct EM simulation of the four baluns. The simulations were done on the baluns including the MIM capacitors. The agreement between measurement and EM simulation for all the baluns is very good; the broadband characteristics of the insertion and return loss closely match the measured data.

V. Conclusion
Modern EM simulators are fast and accurate enough to be used routinely for modeling integrated RF components. We have described the use of such a simulator in several applications: accounting for coupling effects in multi-component designs; analyzing width- and spacing-dependent fabrication effects; and (together with an optimizer) constructing scalable component models. Such models allow fast synthesis of optimal component designs from user specifications.

VI. Acknowledgements
We thank the following companies for the designs and measurements shown in section IV.

- SiGe Semiconductor (www.sige.com) provided the IC diplexer design and measurements.
- Wipro Newlogic provided the integrated VCO design and measurements.
- STATSChipPAC (www.statschippac.com) provided the IPD diplexer design and measurements.
- Taiwan Semiconductor Manufacturing Company Limited (www.tsmc.com) provided the design, fabrication, measurements, and iRCX data for the MoM and stacked inductor examples showing pattern-dependent effects.
- United Microelectronics Corporation (www.umc.com) provided the fabrication and measurements of the baluns.
**Fig. 19.** Inductance, $k$, and Q of the DCS transformer: simulation vs measurement

**Fig. 20.** Insertion loss (IL) and return loss (RL) of baluns: simulation vs measurement

**REFERENCES**


