Optimum Inductor, Capacitor and Transformer Synthesis using EMX and Continuum

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UMC
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Collaboration between UMC and Integrand

- Created industry-first RF/Analog design environment for optimal component design
- Scalable component libraries (130nm, 90nm, 65nm)
  - Planar, symmetric and center-tapped inductors (with PGS)
  - Scalable MOM capacitors (RF and Mixed Mode)
  - Baluns and Transformers
    - Optimum Inductor Finder (OIF)
    - Optimum Capacitor Finder (OCF)
    - Optimum Transformer Finder (OTF)
- Layout and synthesis within UMC’s FDK
  - Uses scalable models of capacitors and inductors
  - Fully integrated within Virtuoso® environment
- EMX integrated within FDK for custom designs
CICC 07 paper on Integrated IC baluns

- Integrate and UMC have published a paper at CICC 2007 titled “Optimal Synthesis of On-Chip Baluns”
- Industry first demonstration of high quality on chip IC baluns.

Synthesis of Optimal On-Chip Baluns


ABSTRACT
We describe a method for synthesizing on-chip baluns. The method involves creating a scalable transformer model from electromagnetic (EM) simulations. Using this model, a quick search through the design space precedes an optimal balun. The search may include constraints such as insertion loss, return loss, area, etc. We used this method to design baluns for common wireless applications. The balun was fabricated in a 0.13 μm CMOS process and measured. The balun had a return loss of about 34 dB and phase imbalance of 5.0° at 2.45 GHz. These characteristics are equal to or better than those of off-chip baluns while requiring significantly less area.

1. INTRODUCTION

Integrated wireless transceivers require a differential circuit architecture. Since balanced E/O connections are commonly single-ended microphone configurations, and antennas are single-ended in nature, many wireless systems require a current balun in the front-end. These are usually implemented as discrete components made with multilayer ceramic or laminate technologies. Conventionally available discrete baluns have about 3-7 dB of insertion loss, up to 20° phase imbalance and up to 180° of phase imbalance.

The feasibility of implementing transformers on IC has long been recognized [7]. However, they are not implemented at the wafer level. A good transformer can provide the following benefits:

- Good phase and amplitude balance
- Good insertion loss
- Good return loss

2. OPTIMAL BALUN SYNTHESIS

The layout of the baluns are designed using an automated layout generator for transformers. The layout of the baluns is shown in Figure 1. The baluns are designed using a commercial software tool.

2.1 Electromagnetic simulation using EMX

We used Electromagnetic simulation software to design a range of geometries with performance criteria: 3-dB bandwidth, height, number of turns, number of dies, number of metal layers, and characteristics of the baluns. We optimized the layout of the baluns using the EMX software.
EMX: “Software Network Analyzer”

Same mask GDSII layout used for wafer fabrication and EM simulation

EMX vs UMC Meas

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EMX

- Electromagnetic simulation
  - Simulation engine for analysis of various passive structures
- EMX is extremely fast and accurate
  - More than 10X faster than other commercial simulators
- Proven silicon accuracy for a very large set of UMC designs
  - inductors
  - capacitors
  - transformers
  - components+interconnect
EMX for UMC structures

\[ E_s(r) = \frac{1}{\sigma} J(r) + j \omega A(r) + \nabla \phi(r). \]

- Physical Effects on ICs
  - R,L,C and Substrate effects unified and fully coupled
- Super-fast Simulation
  - A few minutes for an inductor or a capacitor
- User friendly
  - Processing “true” layout for UMC slotting rules, via arrays, metal fill, and metal biasing for capacitors
- Integrated within UMC’s FDK GUI

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Automated synthesis via scalable models

- **Inductors**
  - 4 types of inductor layouts
  - Planar, Symmetric, Sym CT, stacked
  - Optimize for L and Q

- **Capacitors**
  - 4 types (array and mesh with and without ground shield)
  - Optimize C and Q

- **Transformers, Baluns**
  - 1 type with 4 types of center-tapping
  - Optimize L, Q, Insertion loss
The Optimum transformer finder (OTF)

- Baluns and transformers are important components of RF devices like mobile phones, wireless devices. Used for converting single-ended to differential signal
- UMC and Integrand have collaborated to build transformers and baluns on a 90nm process
- Ceramic Baluns (e.g., Murata, TDK)
  - Insertion loss: 1 – 1.5 dB
  - Phase Imbalance: 10 degrees
  - Amplitude Imbalance: 0.5dB
  - Large Area (2mm x 1.2mm)
  - Off-Chip, large variation and low yield
- UMC Baluns
  - Insertion Loss: 1 - 1.5 dB
  - Phase Imbalance: < 0.25 degrees
  - Amplitude Imbalance: < 0.1dB
  - Small Area (300um x 300um)
  - On-Chip, low variation, high yield, high performance, high integration
EMX vs Measurement for transformers
Design Space and of Transformers

Design Space
nt_in: 1 to 9 turns
nt_out: 1 to 9 turns
turns ratio: 1:1, 1:2, 1:3, 1:4
w: 3 to 12 µm
s: 2µm µm
od: 75 to 300 µm
f: DC to 20 GHz

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Inductance Mode (Forward)

1. Select mode
2. Type in Geometric Parameters
3. Obtain Electrical Parameters
Inductance Mode (design)

4) Give Electrical Parameters
   - Give L1 inductance
   - Give a range for L2
   - Bandwidth? Delta?

5) Obtain Geometric Parameters of an optimal transformer

OTF automatically minimizes the area?
Inductance Mode (plot)
Losses Mode

- This is the mode that most designers will use the OTF.
- In this mode the designer specifies the input and output impedances, e.g.,
  - Input impedance of package
  - Output impedance of driver
- The OTF then finds
  - the optimum transformer
  - associated tuning MiM capacitors that will satisfy the loss constraints
- The most important design is a balun which has a single-ended input and a differential output
  - Example using \texttt{L\_Transformer\_ctout\_RFVIL}
  - Primary is not center-tapped
  - Secondary is center-tapped
Designing an 802.11B balun (2.5GHz) using losses mode

- Design a single-ended to differential balun with center-tapped output using the following constraints
  - 50 Ohms input impedance
  - 200 Ohms output impedance
  - Minimum insertion loss of –1dB
  - Maximum return loss of –10dB
- OTF determines
  - Balun geometry
  - Input and Output MiM capacitor values to tune the balun
  - Minimize area (including MiM area)
Plotting insertion and return losses
Schematics for 4 types of transformers

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Balun silicon verification (Insertion Loss)

802.11A

802.11B

DCS

GSM

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Phase and Amplitude imbalance

802.11A
- Phase Imbalance vs. GHz
- Amplitude Imbalance vs. GHz

802.11B
- Phase Imbalance vs. GHz
- Amplitude Imbalance vs. GHz

UCS
- Phase Imbalance vs. GHz
- Amplitude Imbalance vs. GHz

GSM
- Phase Imbalance vs. GHz
- Amplitude Imbalance vs. GHz

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LKQ plots

802.11A

\[ k - \frac{L1}{\sqrt{L1^2 + L2^2}} \]

802.11B

\[ k - \frac{L1}{\sqrt{L1^2 + L2^2}} \]

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LKQ plots

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New Advanced model features

- Advanced features have been added to the scalable models for UMC
- These new features were based on measurements
  - The models now include temperature dependence
  - The models include the ability to handle Monte-Carlo statistics on process variation
Temperature coefficient extraction

Temp coefficient=(percent change in resistance)/degree

<table>
<thead>
<tr>
<th>Structure</th>
<th>Temperature coefficient</th>
</tr>
</thead>
<tbody>
<tr>
<td>IND905</td>
<td>0.46</td>
</tr>
<tr>
<td>IND914</td>
<td>0.48</td>
</tr>
<tr>
<td>IND916</td>
<td>0.54</td>
</tr>
<tr>
<td>Pure copper (theory)</td>
<td>0.4</td>
</tr>
</tbody>
</table>

Temperature coefficients extracted from Inductor measurements
Temperature dependence in EMX: IND905

Substrate Temp Coefficient of 0.35: IND905
Monte-carlo statistics

- Inter-wafer statistical variation was studied

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Monte-carlo scalable model results

- Monte-carlo statistics extracted from the measurements has been included in the scalable models.
Summary

- Successful and ongoing collaboration between UMC and Integrand Software Inc.
  - OIF (Inductors with and without PGS)
  - OCF (Capacitors for RF and Mixed-mode applications)
  - OTF (Transformers and Baluns)
- Extended the functionality of UMC’s FDK
  - Process variation effects in scalable models
  - Temperature dependence in models
  - Capacitor Mismatch
Extra Slides
Inductors: EMX Simulation vs. Measurement

**IND803 umc013-nwell-G13409**

\begin{align*}
L & : 
\begin{array}{c}
0.6 \\
1 \\
1.2 \\
1.4 \\
1.6 \\
0 \\
5 \\
10 \\
15 \\
20 \\
\end{array} \\
Q & : 
\begin{array}{c}
0 \\
5 \\
10 \\
15 \\
20 \\
0 \\
5 \\
10 \\
15 \\
20 \\
\end{array} \\
R & : 
\begin{array}{c}
0 \\
10 \\
10^1 \\
10^2 \\
10^3 \\
0 \\
5 \\
10 \\
15 \\
20 \\
\end{array} \\
Z & : 
\begin{array}{c}
1 \\
10 \\
10^1 \\
10^2 \\
10^3 \\
0 \\
5 \\
10 \\
15 \\
20 \\
\end{array} \\
\end{align*}

**IND803 umc013-psub-G13409**

\begin{align*}
L & : 
\begin{array}{c}
0.9 \\
1 \\
1.1 \\
1.2 \\
1.3 \\
0 \\
5 \\
10 \\
15 \\
20 \\
\end{array} \\
Q & : 
\begin{array}{c}
0 \\
5 \\
10 \\
15 \\
20 \\
0 \\
5 \\
10 \\
15 \\
20 \\
\end{array} \\
R & : 
\begin{array}{c}
0 \\
10 \\
10^1 \\
10^2 \\
10^3 \\
0 \\
5 \\
10 \\
15 \\
20 \\
\end{array} \\
Z & : 
\begin{array}{c}
1 \\
10 \\
10^1 \\
10^2 \\
10^3 \\
0 \\
5 \\
10 \\
15 \\
20 \\
\end{array} \\
\end{align*}

**IND804 umc013-psub-G13409**

\begin{align*}
L & : 
\begin{array}{c}
1.5 \\
2 \\
2.5 \\
3 \\
3.5 \\
0 \\
5 \\
10 \\
15 \\
20 \\
\end{array} \\
Q & : 
\begin{array}{c}
0 \\
5 \\
10 \\
15 \\
20 \\
0 \\
5 \\
10 \\
15 \\
20 \\
\end{array} \\
R & : 
\begin{array}{c}
0 \\
10 \\
10^1 \\
10^2 \\
10^3 \\
0 \\
5 \\
10 \\
15 \\
20 \\
\end{array} \\
Z & : 
\begin{array}{c}
1 \\
10 \\
10^1 \\
10^2 \\
10^3 \\
0 \\
5 \\
10 \\
15 \\
20 \\
\end{array} \\
\end{align*}

**IND804 umc013-nwell-G13409**

\begin{align*}
L & : 
\begin{array}{c}
1.6 \\
2 \\
2.5 \\
3 \\
3.5 \\
0 \\
5 \\
10 \\
15 \\
20 \\
\end{array} \\
Q & : 
\begin{array}{c}
0.9 \\
1 \\
1.1 \\
1.2 \\
1.3 \\
0 \\
5 \\
10 \\
15 \\
20 \\
\end{array} \\
R & : 
\begin{array}{c}
0 \\
10 \\
10^1 \\
10^2 \\
10^3 \\
0 \\
5 \\
10 \\
15 \\
20 \\
\end{array} \\
Z & : 
\begin{array}{c}
1 \\
10 \\
10^1 \\
10^2 \\
10^3 \\
0 \\
5 \\
10 \\
15 \\
20 \\
\end{array} \\
\end{align*}
MOM Capacitors

- UMC MOM capacitors are accurately simulated by EMX
- Need true 3D simulation capabilities to handle metal sidewall and via sidewall capacitance
- EMX automatically handles vias, metal bias that can affect the capacitance value
MOM Capacitors: EMX Simulation vs. Measurement

CAP305+GSG

CAP404+GSG

CAP314+GSG

CAP413+GSG
Scalable Component Models

- “Scalable” Models of Inductors and Capacitors
  - Spice models parameterized by geometry
  - Critical for foundry model libraries
  - Created using EMX and Continuum
Design Space of Inductors

Design Space
nt: 1.5 to 7.5 turns
w: 3 to 10 µm
s: 1.5 to 5 µm
od: 75 to 300 µm
f: DC to 20 GHz

\[ L_c = f_1(w, od, nt, s) \]
\[ C_{sub1} = f_2(w, od, nt, s) \]
\[ R_{sub2} = f_3(w, od, nt, s) \]

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Design Space of Capacitors

**Design Space**
- nf: 7 to 101 fingers
- Metal stack: 3 to 6 layers
- Length: 5 to 25 µm
- Array: 1 to 4x
- f: DC to 20 GHz

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EMX-Continuum™

- Scalable Model Generator
  - Discretization of space
  - Built from 1000s of individual component (inductor or capacitor) simulations
  - EMX as simulation engine
  - Proprietary techniques used to develop “unified” model
  - Pure RLCK Spice
  - Passive by construction
  - Noise analysis correct

Design Space
nt: 1.5 to 7.5 turns
W: 3 to 10 µm
S: 1.5 to 5 µm
OD: 75 to 300 µm

Layout generator
(UMC Cadence PCELL)

EMX-Continuum

Spice Models
Spectre, Eldo, Hspice, ADS
The Optimum Inductor Finder (OIF)

- Design Space Optimization
  - Finding optimal inductor design
  - Using the scalable spice models
  - Almost instantaneous playback (5~10 seconds)
  - GUI interface in Cadence Virtuoso

- Optimizations
  - Maximize Q
  - Minimize Area
  - Bandwidth optimizations
  - Including PGS
Optimal Inductor Design for UWB

Trading Q for consistent inductance over wide bandwidth

The goal of UWB design is to “flatten the inductance”
Typical Model Accuracy
PGS Design

- PGS capabilities added
- Patterned ground plane shields substrate
- Can increase Q by 30%
- 3 PGS models (planar, symmetric, center-tapped) added to the UMC FDK
UMC’s FDK with the Optimum Inductor Finder

OIF

Layout View

Symbol View
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Scalable Spice Model
Optimum Capacitor Finder (OCF)

- Determine optimal capacitor design based on a number of tradeoffs:
  - Area
  - Q
  - Space/Shape Constraints
  - Metal Stacks
- Single-ended or Differential Design
OCF for RF Applications

Plotting

Layout

Schematic

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4 Mixed-mode Capacitors
Common Centroid Design of Capacitors

Common Centroid Design minimizes the effect of mismatch
EMX direct interface to UMC’s Design Kit

- It is possible to directly access EMX through the UMC FDK (in Virtuoso®)
- Allows designers to design components not contained in UMC library
- Simulation of components and surrounding interconnects (proximity effects)

Use the EMX menu to start the simulation window