PRO FOUNDRY

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Letter From the CEO

HIGHLIGHTS

COMPANY NEWS

DESIGN NEWS

UMC
THE SoC SOLUTION FOUNDRY

"For the quarter, 90nm shipments contributed to 14% of the quarterly revenue. New 90nm customers continued to make good progress. Some of them have achieved successful prototypes and have started the qualification process."

Dr. Jackson Hu, CEO, UMC

2005 is drawing to a close, giving us the opportunity to reflect on a year that was both challenging and rewarding. UMC recently announced its latest quarterly earnings, and we successfully accomplished our operating goals for Q3. Revenue growth was 21.3% higher than Q2 while utilization rate improved to 78%. Operating loss for the quarter was greatly reduced from NT$3.34 billion in Q2 to NT$580 million. In September, we actually returned to profitability on a monthly basis. Revenue from 90nm products contributed significantly to this turnaround. By the end of September, accumulated shipments reached 118K 8" equivalent wafers. For the quarter, 90nm shipments contributed to 14% of the quarterly revenue. New 90nm customers continued to make good progress. Some of them have achieved successful prototypes and have started the qualification process. We expect that these customers will begin production in the next few months. When this happens, it will greatly improve our technology mix, i.e., the percentage of revenue contribution from advanced technologies will improve significantly. Furthermore, these high-volume customers will also improve our application mix and enhance UMC's long-term business stability.

On the new technology development front, we are continuously making good progress in new design wins. Today, we have four customers doing prototype

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development on 65nm. We expect to pass qualification and start small volume production for one customer in Q1 2006.

Within our visibility, Q4 will be another high growth quarter. Wafer shipments are estimated to increase by low teen percentage points. Revenue growth will be between 15-20%. Capacity utilization will increase to 85%. Quarterly, we will be profitable. 0.18um and smaller geometries will contribute 67% of revenue, while 90nm will be in the high teen percentage range. Application wise, the communication sector is expected to be the strongest followed by the computer and consumer segment. 2005 Capex budget will stay at $1B. It is worthwhile to point out that Q4 revenue will peak in November, as we noticed that some customers became more conservative in their December forecasts. It is likely that many customers are watching for the holiday sell-through situation. This may prevent inventory build-up and is considered as a positive sign.

In the meantime, we have introduced many new SoC solutions to assist designers on their road to product success. Some of the highlights can be found in this latest issue of ProFoundry, which I hope you will enjoy.

PF

UMC Sponsors FSA Suppliers Expo Taiwan as Platinum Sponsor

UMC supported FSA's November 2 Suppliers Expo in Taiwan as a Platinum sponsor, the highest level of sponsorship. The event featured speakers from experts across the industry and drew over 1000 attendees. UMC joined more than 50 other companies with its own booth at the exhibition where guests had the opportunity to speak with UMC engineers about the latest SoC solution offerings available to UMC customers.

UMC is also supporting the FSA Awards Dinner on December 8, 2005 in Santa Clara as the sole Title Sponsor for the event.

ABOUT THE FSA

FSA is the voice of the global fabless business model. Industry leaders incorporated FSA in 1994 on the premise that the fabless business model would be a viable, long-term business model. Today, the viability of outsourcing as a sustainable business model for the industry has been proven, and FSA is focused on the perpetuation of this business model throughout the worldwide semiconductor industry.

PF

UMC Europe Relocates Office to WTC Schiphol Amsterdam Airport

On September 14, 2005, UMC Europe (BV) celebrated its move to the WTC Schiphol Amsterdam Airport in the Netherlands with a grand opening ceremony at its new office. The ceremony was led by UMC executives, who were joined by Mr. A.A.M. van Agt, former Dutch Prime Minister, Mrs. S.Y.Chang, Taiwan's representative in the Netherlands, Dr. Benno Fritzler, Infineon Vice President of Silicon Foundry, Mr. Nik Kaeppeler, Micronas COO, Mr. Pieter Verboom, CFO Schiphol-group, and Mr. Hans Zwarts, President of the Chamber of Commerce of Amsterdam.

UMC's customer base in Europe includes leading major high-tech companies such as Infineon, STmicroelectronics, Philips and Micronas.

The grand opening was attended by over 60 customers, government officials and representatives of various UMC partner organizations. The morning consisted of an opening reception party, ribbon cutting ceremony, and traditional Chinese Lion dance, followed by a customer testimonial program with Infineon, Micronas, IMEC/Europractice and Moscad contributing.

The ultra-modern airport facility will allow UMC to much more efficiently serve its European customers as those flying to UMC Europe from other parts of the world will conveniently find the brand new office located right on the airport grounds.

UMC was one of the first Taiwan-based companies to establish its European headquarters in Amsterdam when it first opened its offices there in 1989. Since then, UMC has grown to become the largest foundry supplier in Europe with over $500 million in sales coming from its UMC Europe BV offices in 2004.

UMC Europe BV: New Office Address

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RAMBUS AND UMC EXPAND AVAILABILITY OF RAMBUS PCI EXPRESS PHY IP TO UMC'S 90NM PROCESS

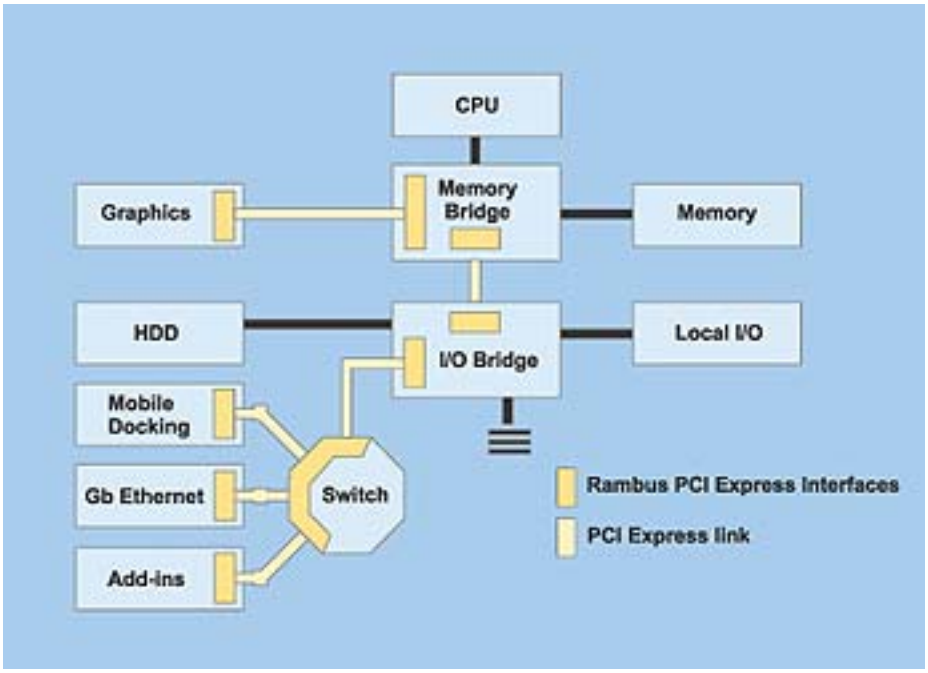
Rambus Inc. and UMC have extended the availability of Rambus's patented PCI Express PHY cells to now include UMC's 0.18um, 0.15um, and 90nm processes. This development expands on the existing 0.13um licensing agreement between the two companies, which was signed in 2004. UMC is currently manufacturing several high-volume customer products with Rambus's PCI Express PHY cells.

Under the agreement, UMC foundry customers gain access to Rambus's broad portfolio of PCI Express-based interfaces. The Rambus PCI Express PHY cells have been designed to provide chip developers with a solution that optimizes link utilization, latency, power consumption and silicon footprint. The PCI Express interface standard is one of the industry's most successful for chip-to-chip interconnects and can be found in system applications ranging from supercomputers to PCs and digital TVs.

Rambus PCI Express PHYs are complete serial communication cells optimized for implementing the physical layer of the PCI Express standard. The silicon-proven serial interfaces feature point-to-point, full duplex signaling and support up to a 3.2Gbps data rate.

Rambus has also demonstrated its Turbo PCI Express platform with serial links operating at 5.0Gbps and 6.25Gbps data rates to meet future PCI Express requirements. Rambus PCI Express PHYs are listed on the PCI-SIG Integrators List, having passed PCI-SIG compliance and interoperability testing by Rambus PHY cell customers and digital controller partners.

The PCI-SIG is the special interest group that owns and manages PCI specifications as open industry standards. The Rambus PCI Express PHY cells are supported by a comprehensive suite of digital controllers and support services to provide chip developers with a complete system solution. For more information on Rambus's broad PCI Express offering, visit www.rambus.com/products/pciexpress. PF



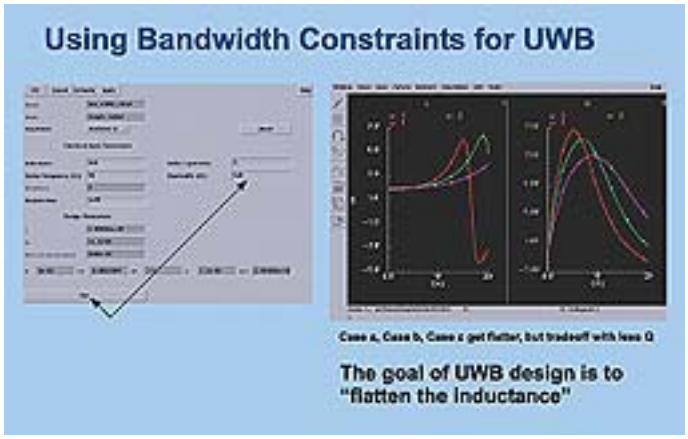
Rambus PCI Express Serial Link Applications

UMC and Integrand Bring Advanced Capabilities to 0.13um RFCMOS Designers

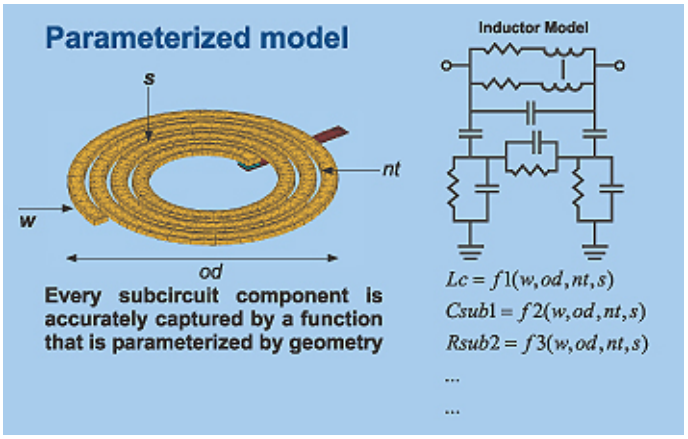
UMC and Integrand Software, Inc., have collaborated to develop leading edge, IC design resources for 0.13um RF designers. Through the partnership, UMC's Virtual Inductor Library (VIL) is more robust and has new capabilities from Integrand tools. A new graphical user interface (GUI) tied to UMC's Foundry Design Kit (FDK) gives designers the means to create accurate designs in a shorter amount of time.

Integrand's EMX® and EMX-Continuum™ tools, utilized in UMC's VIL, have been used for the synthesis of Spice models for a variety of spiral inductors, including Planar, Stacked and Symmetric inductors. Accuracy has been verified to be within a few percent of measurements for inductance, as well as for more sensitive parameters like the quality factor (Q).

Traditionally, scalable models have been provided by foundries only for active components. The EMX-Continuum software was used to create true parameterized, or scalable, models for UMC's spiral inductors. In addition, Integrand's Optimum Inductor Finder™ combined with UMC's FDK and VIL represent a unique solution to the inductor synthesis problem, previously thought intractable because of the large design space of passives.



Integrand's Optimum Inductor Finder, a GUI-based synthesis tool, is now deployed within the FDK to allow UMC customers to enter their desired inductance and make tradeoff decisions between Q and area. Designers may also request a specified "flatness" of inductance within a given frequency range for Ultra-Wideband (UWB) circuit designs. The seamless integration within the FDK allows for back annotation in order to drive UMC's Schematic Driven



Layout. Furthermore, the Spice model parameters are geometric to allow EDA Layout Parasitic Extraction (LPE) tools to extract model parameters from a GDS database for post-layout simulation. In addition, with the new Optimum Inductor Finder GUI, it takes just a few seconds for designers to create an optimal inductor, a capability that significantly increases the likelihood of first-silicon success without extending design cycle time for 0.13um RFCMOS designs.

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Project Highlights:

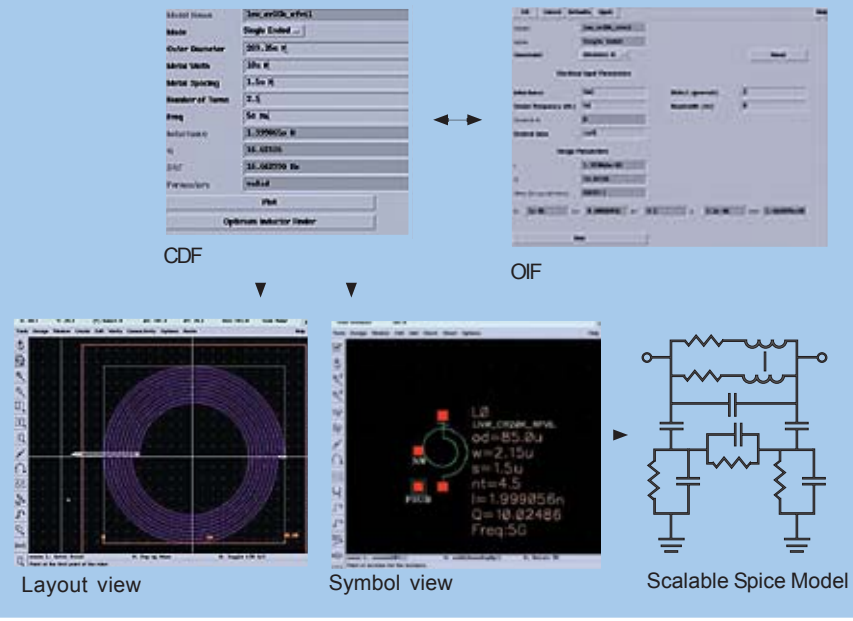
EMX-Continuum: UMC used the EMX-Continuum software to create scalable inductor models that have several important features:

- The scalable models are standard RLCK Spice; this guarantees correct noise modeling when doing Spice-level simulation.
- The models are available in Spectre®, ELDO®, ADS and HSPICE® format.
- The models are directly interfaced to the Optimum Inductor Finder GUI deployed with the FDK.
- The Optimum Inductor Finder back-annotates the results to allow schematic driven layout.

EMX: EMX is based on the Fast Multipole method combined with a patent-pending approach to recognize geometric regularity in IC layouts for efficient electromagnetic (EM) simulation. EMX exhibits several important features:

- UMC has found that the simulation of its inductors takes only a couple of minutes for a full broadband sweep.
- EMX was useful for designing patterned ground shields, resulting in an increase in Q of about 35% for some inductors (verified by measurement).
- EMX has been used for the design of optimal deembedding designs for Open and Short structures.
- EMX works directly off the final mask layout and handles features of UMC's layouts such as slotting rules and via arrays with no manual editing. PF

UMC's FDK with the Optimum Inductor Finder



UMC Introduces 90nm Reference Design Flow

UMC has released a comprehensive reference flow for 90nm system-on-chip (SoC) designs. The silicon verified RTL-to-GDSII flow is based on UMC's 0.13um low-power design package, and incorporates timing closure, signal closure, and power closure features to help SoC designers overcome 90nm design-related challenges. Moreover, the added dimension of the latest design for manufacturing (DFM) rules applied within the reference flow provides designers with new capabilities to achieve accurate, first-time-right designs and shortened time-to-market.

SoC designers today require proven design support solutions to help them overcome the challenges of 90nm and below technologies. The availability of this newest, comprehensive reference flow promises to help customers navigate the most seamless path to 90nm silicon success by providing a feature rich solution that is supported by the latest EDA tools and DFM methodologies.

The design flow focuses on improving DFM issues by applying DFM-aware technology files at strategic areas of the flow. DFM

UMC Introduces Industry's Most Comprehensive Low-Power Design Package

UMC recently introduced the industry's most comprehensive low-power reference design package to specifically target the needs of low power, system-on-chip (SoC) designers. The offering delivers a fast, more predictable path to silicon success and sets a new precedent in the foundry industry in terms of providing customers with a complete solution to help shorten their product development time for low power designs. This technology enabler for nanometer designs is available for UMC's 0.13um process today, and includes:

- Silicon-verified test chip that features the open-source LEON2 SPARC processor
- Process optimized low-power libraries
- Low power technology files
- Integrated RTL-to-GDSII reference flow incorporating the latest tools from Cadence Design and Mentor Graphics

As designs scale to smaller process technologies, leakage and other power challenges become bigger obstacles for SoC designers. To effectively address these issues, designers need a total package solution that will help guide them efficiently through the design process. The delivery of this comprehensive offering provides designers with key resources to help them quickly and successfully bring their low-power ICs to market

The reference design package expands well beyond a typical foundry reference flow to also include a host of other silicon-verified resources developed to work together. Low power SoC developers can reference the test chip that includes a LEON2 processor-the open source synthesizable VHDL model of a 32-bit processor, while designing their own SoC designs. The chip design is highly configurable and expandable, allowing customers to plug in additional digital and/or analog/mixed signal (AMS) hard IP blocks, making it ideal for specific derivative designs that customers are

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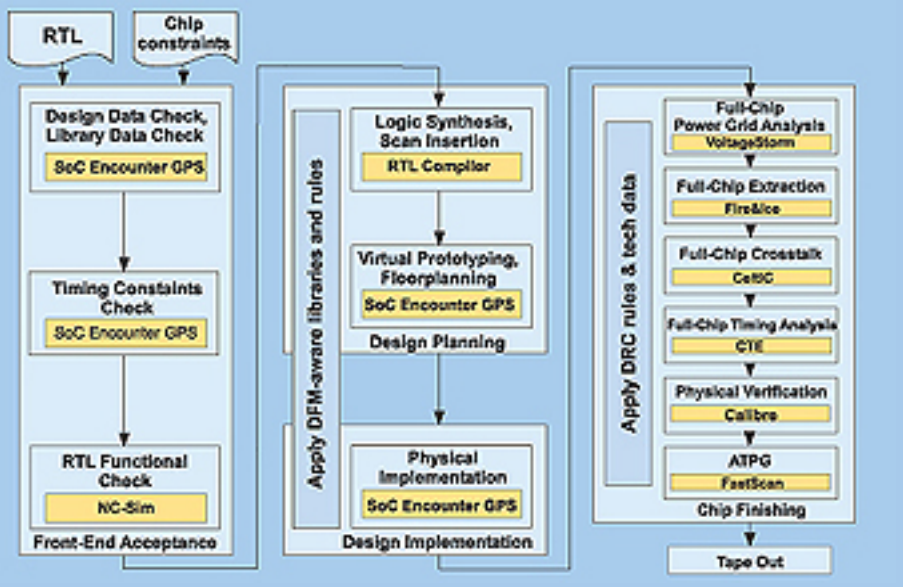
rules and technology data are incorporated into libraries in both front-end and back-end views; thus, the entire design flow has taken DFM into consideration.

To validate the 90nm flow, UMC utilized its 0.13um LEON2 CPU based technology demonstrator as a reference design to implement a top-down solution for the RTL-to-GDSII design flow. Design for test (DFT) and design for diagnosis (DFD) elements are featured to ensure design accuracy. The reference flow is available now for download at www.umc.com.



Overview of UMC's 90nm Reference Design Flow

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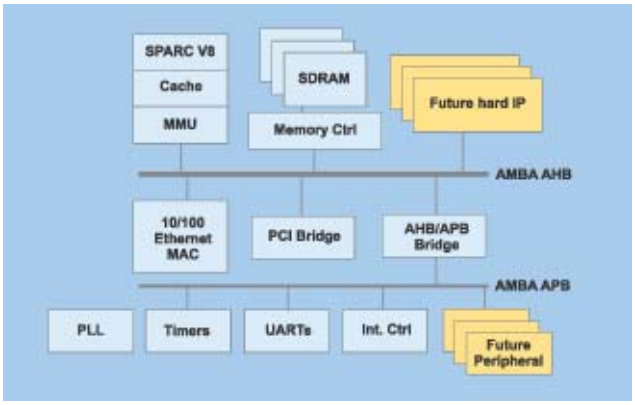
evaluating. The chip can also be used for greater insight into the process or device side effects of advanced technology and to figure out solutions, set up a library and IP QA methodology through chip implementation, and validate process, library, IP, and EDA tools and flow before adoption.

The silicon-validated reference flow adopts the Cadence Encounter digital IC design platform, which includes Encounter RTL Compiler synthesis, SoC Encounter Global Physical Synthesis (GPS), VoltageStorm static and dynamic power analysis, and CeltIC Nanometer Delay Calculator (NDC). For design-for-test (DFT), it adopts the latest Mentor flow, which integrates MBISTArchitect, DFTAdvisor and TestKompress and for physical verification uses Mentor's Calibre tool. The reference flow provides the user with an understanding of the low-power design flow and in-depth DFT using the LEON2 based test chip as a reference design.

Silicon-proven libraries and technology files complete the low-power reference design package, and provide the basic building blocks for customers to begin their low-power SoC development. Customers interested in this offering should contact their UMC sales representative. PF



UMC's low power package includes the Leon2 technology demonstrator

New Customers
For new customer inquiries, please direct all questions to sales@umc.com

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