Optimum Spiral Inductor Synthesis for UMC's Virtual Inductor Library using EMX®

Integrand Software Inc.

www.integrandsoftware.com

Integrand Software, Inc.

UMC

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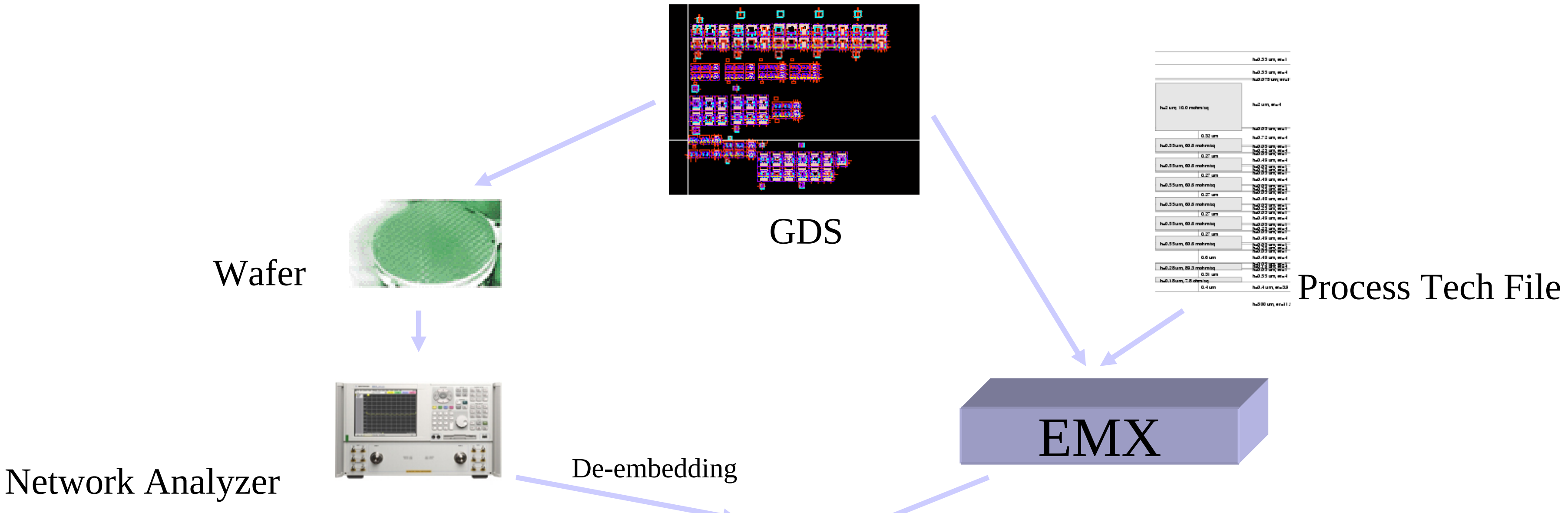
Outline

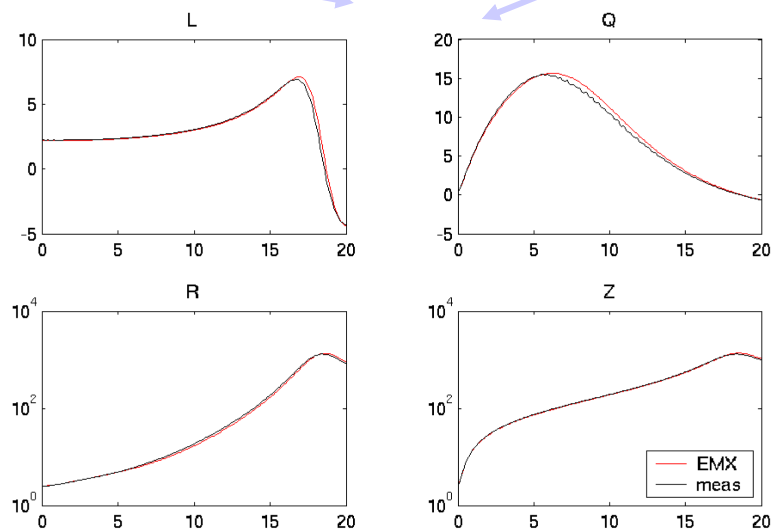
- Collaboration between UMC and Integrand
  - Industry first "virtual" inductor library for 0.13um
  - Scalable models and synthesis tools within FDK
- EMX®
  - electromagnetic simulation of passives
- EMX-Continuum™
  - scalable models of spiral inductors
- The Optimum Inductor Finder™
  - Layout synthesis within Cadence Virtuoso® environment
  - Enabled by cadence CONNECTIONS

EMX

- Electromagnetic simulation
  - Simulation engine for analysis of passive structures
  - DAC 2004
    - S. Kapur and D. E. Long, *Large-scale full-wave simulation*, pp 806-809.
  - EMX is extremely fast and very accurate
    - 10X-100X faster than other commercial simulators
- Distinguishing features
  1. Electromagnetics (accuracy)
  2. Numerical Analysis (speed)
  3. Software (user friendly)

"EMX: Software Network Analyzer"





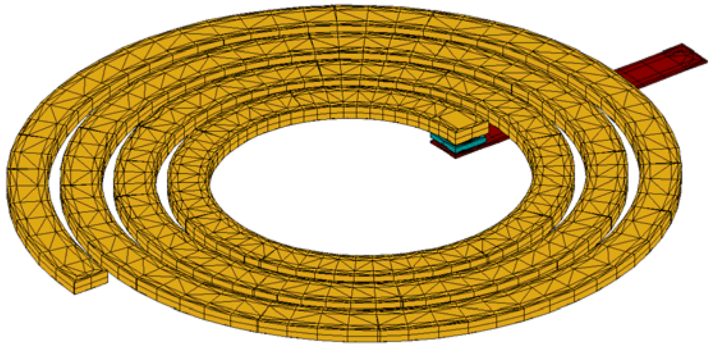
EMX vs UMC Meas

Same mask GDSII layout used for wafer fabrication and EM simulation

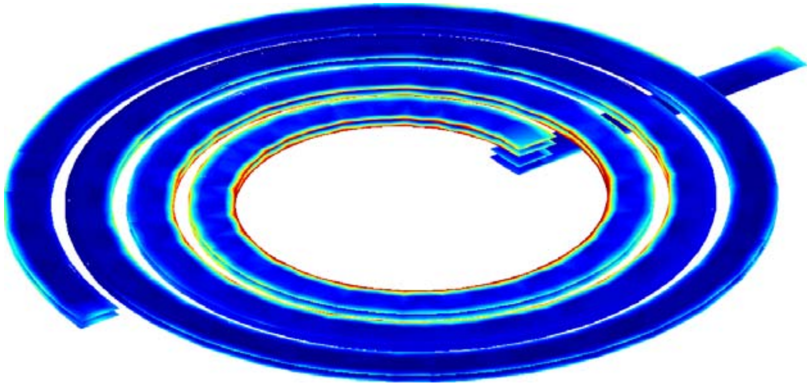
Electromagnetics (accuracy)

$$E_s(r) = \frac{1}{\sigma} J(r) + j\omega A(r) + \nabla\phi(r).$$

- Physical Effects on ICs
  - R,L,C and Substrate effects unified and fully coupled
- Inductance
  - Distributed 3D volume currents
- Resistance
  - Skin effect and volume loss
- Capacitance
  - Accurate sidewalls MOM caps
  - Thin-film MIM caps
- Substrate
  - Multi-layered lossy substrates
  - Substrate doping and bias



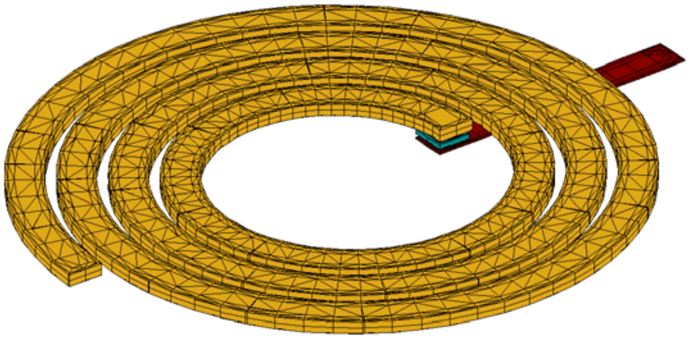
3D mesh of UMC inductor



Current Flow

Numerics (speed)

- Integral Equation Based 3D EM field solver
  - Preconditioned Iterative methods
  - New "Full-Wave" FMM
  - Layout-regularity exploiting
  - Adaptive Fast Frequency Sweep using Krylov Subspace techniques
- Speed
  - 2 orders of magnitude faster than finite-element, 1 order faster than BEM



UMC inductor

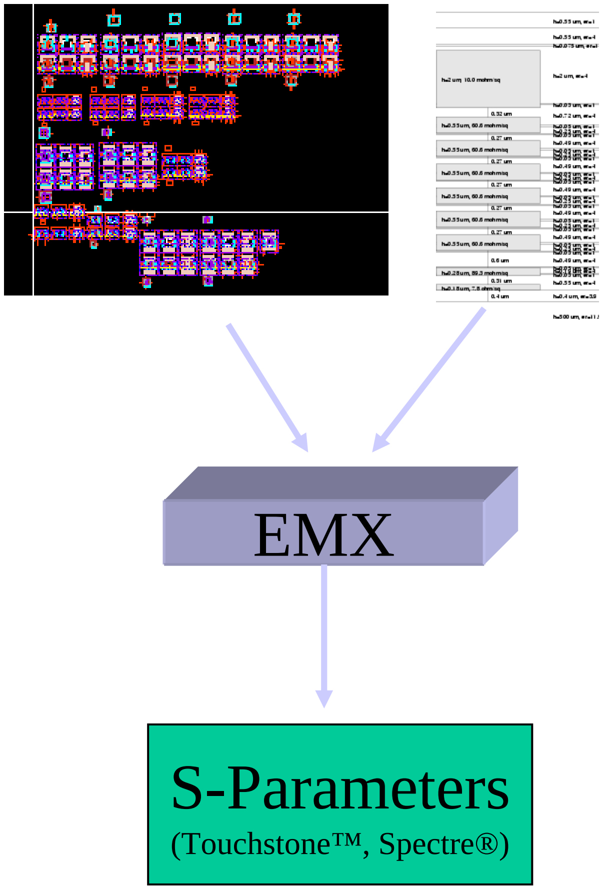
9244 basis functions
13692 vector potential elements
4877 scalar potential elements

Freq Range	Frequencies	Time	Memory
5 GHz	1	40 sec	7 MB
0.1 to 20 GHz	Sweep (201)	90 sec	22 MB

AMD Athlon XP 3200
2.2 GHz, 1G RAM

Software (user friendly)

- Processing “true” layout for UMC
  - 0.13um slotting rules, via arrays, metal fill
  - Context dependent vias (m1, poly)
  - Automatic growing/shrinking of layout geometry for scaling/bias and statistical analysis
  - Simply write scripts or programs to do 1 or 10s of simulations at a time
- Extensively used at UMC for
  - Inductors/Transformers/Capacitors
  - Open/Short De-embedding Structure Improvement
  - Coupling Analysis
  - Substrate Analysis



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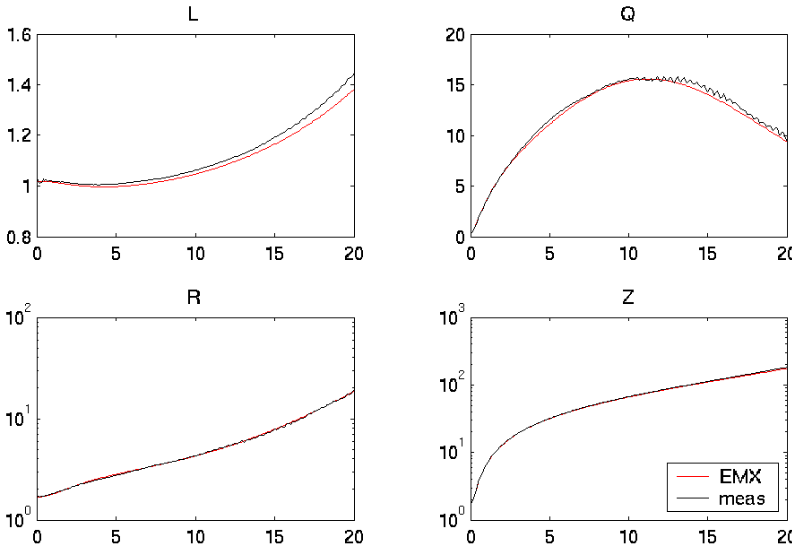

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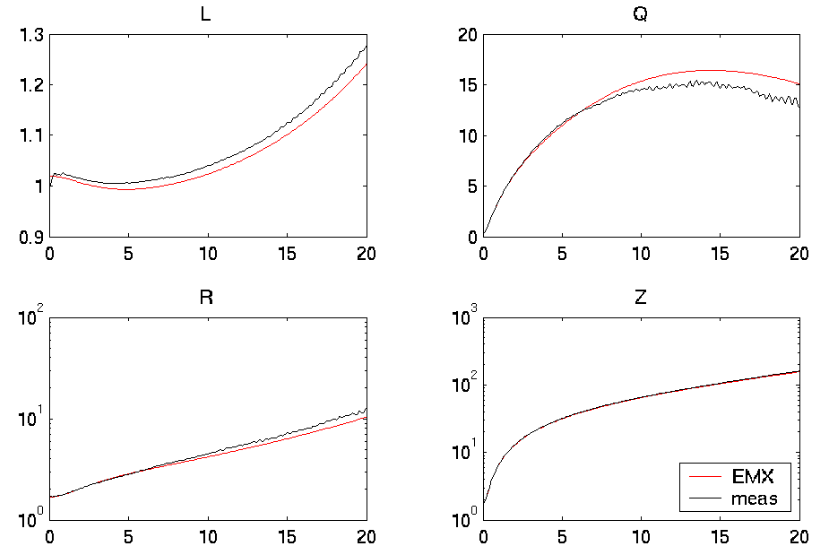

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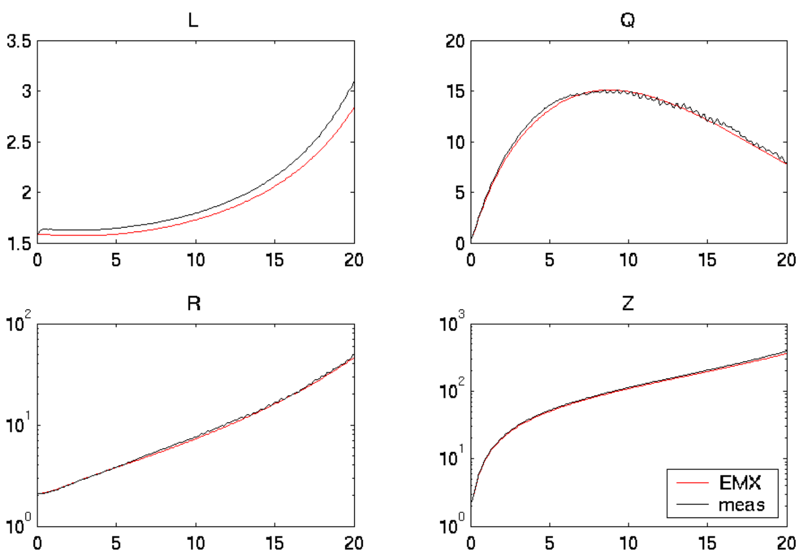

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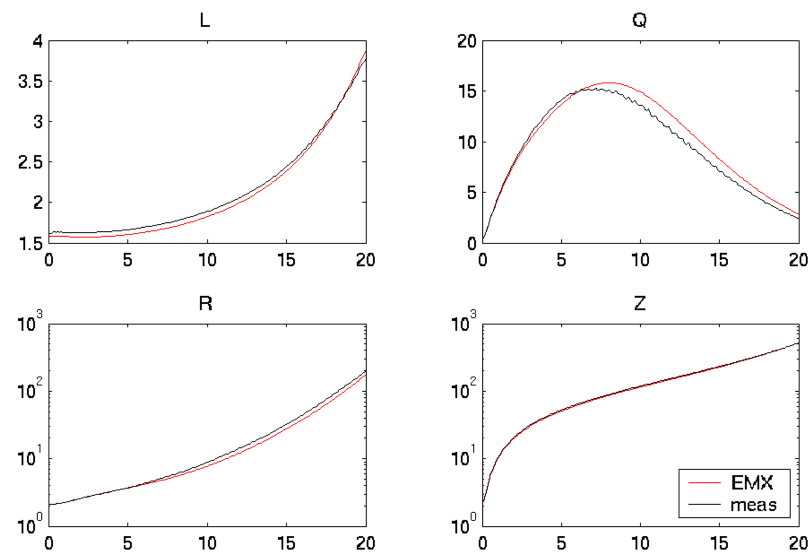

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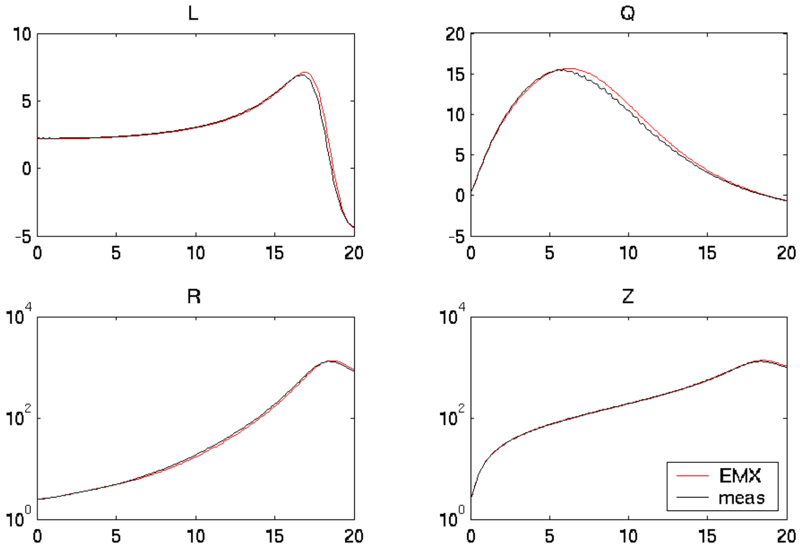

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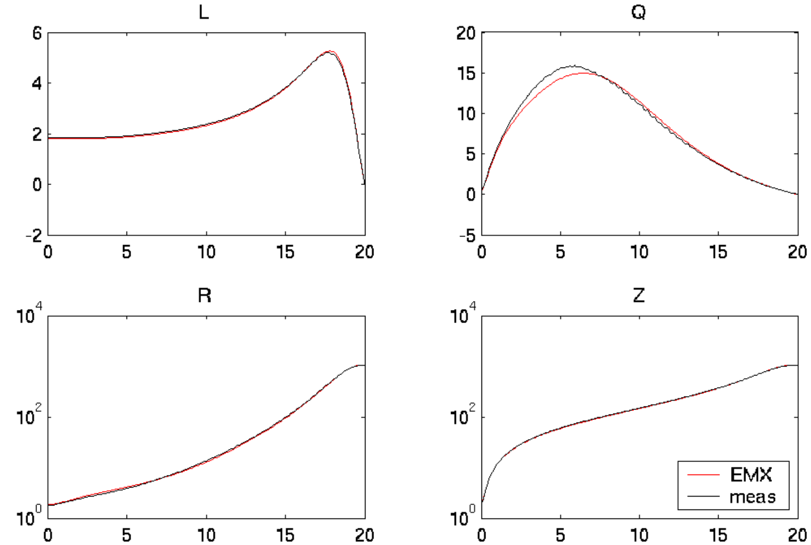

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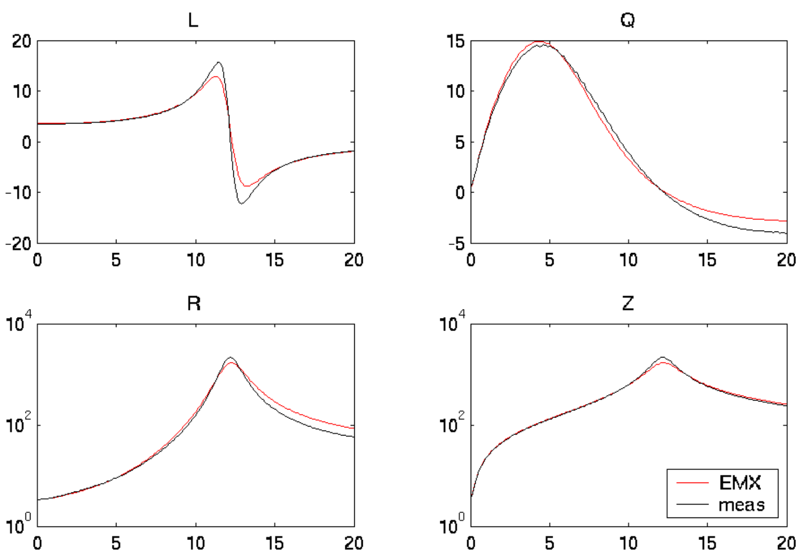

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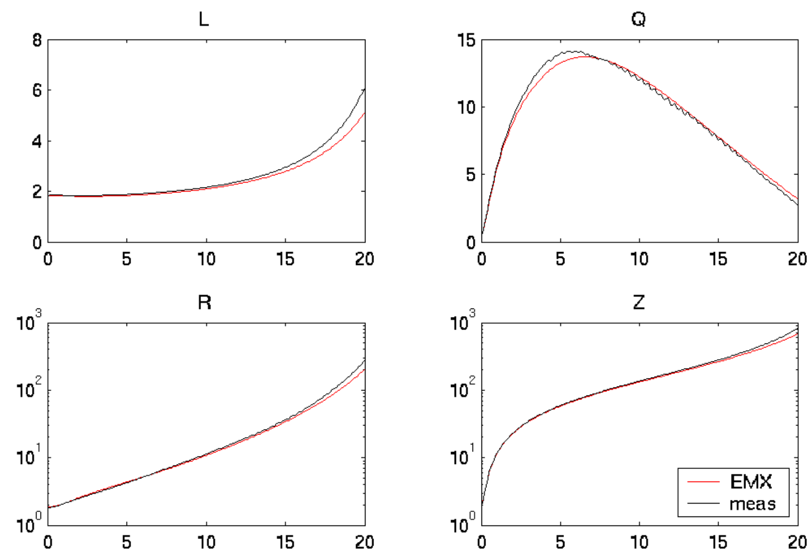
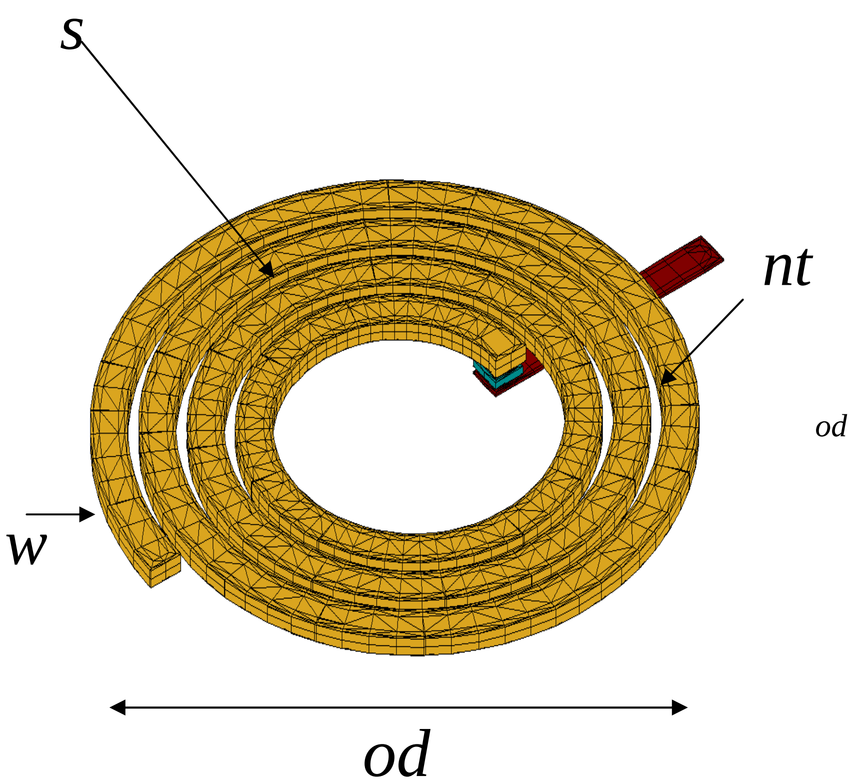
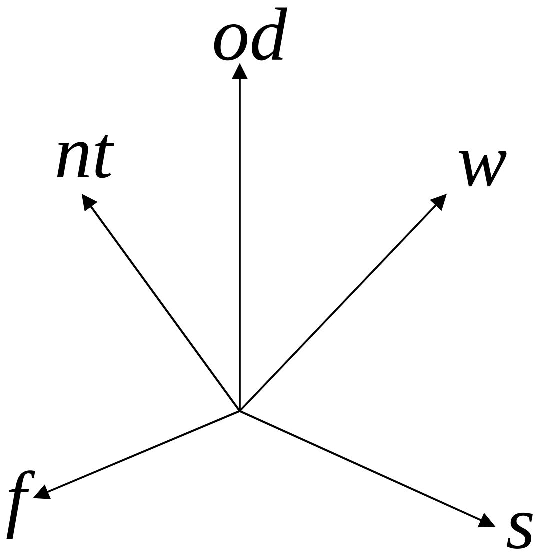


Scalable Models

- "Scalable" Models of Inductors
  - Spice models parameterized by geometry
  - Critical for foundry model libraries
- Traditionally
  - Active devices (simple geometry, MOSFET)
  - Simple passives (plate capacitors, A/d)
  - Either not done for inductors or done "poorly"
  - Conventional Wisdom: Inductor models are difficult to parameterize due to large design space

Design Space of Inductors

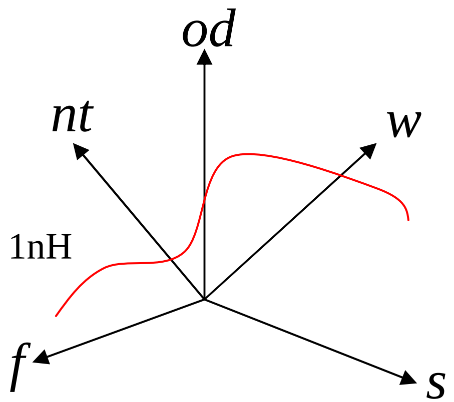


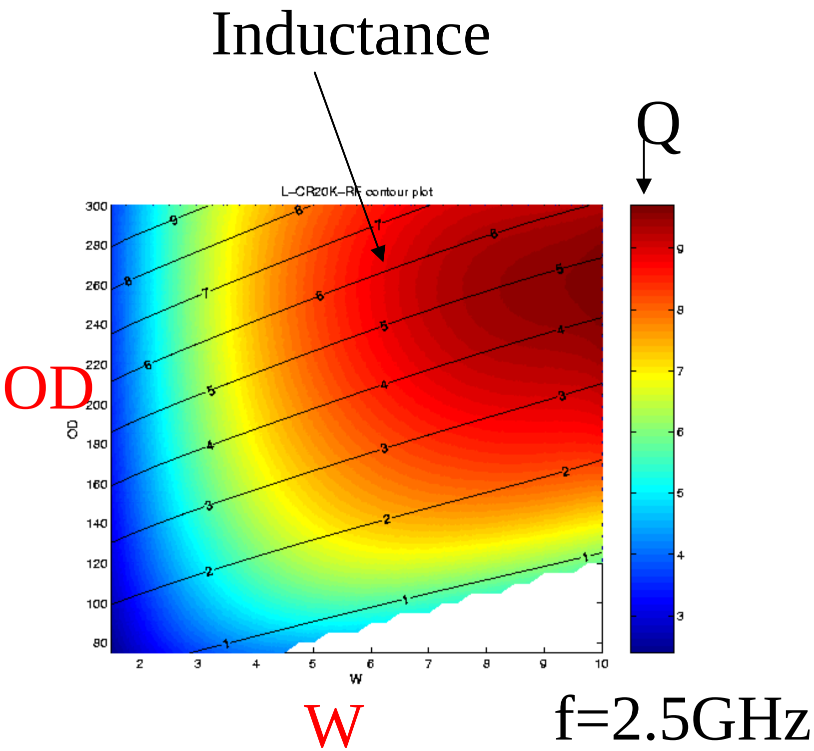


- Design space is large (5D)
- Covers every conceivable inductor

Design Space
nt: 1.5 to 7.5 turns
w: 3um to 10um
s: 1.5um to 5um
od: 75um to 300um
f: DC to 20GHz

Smoothness of Space



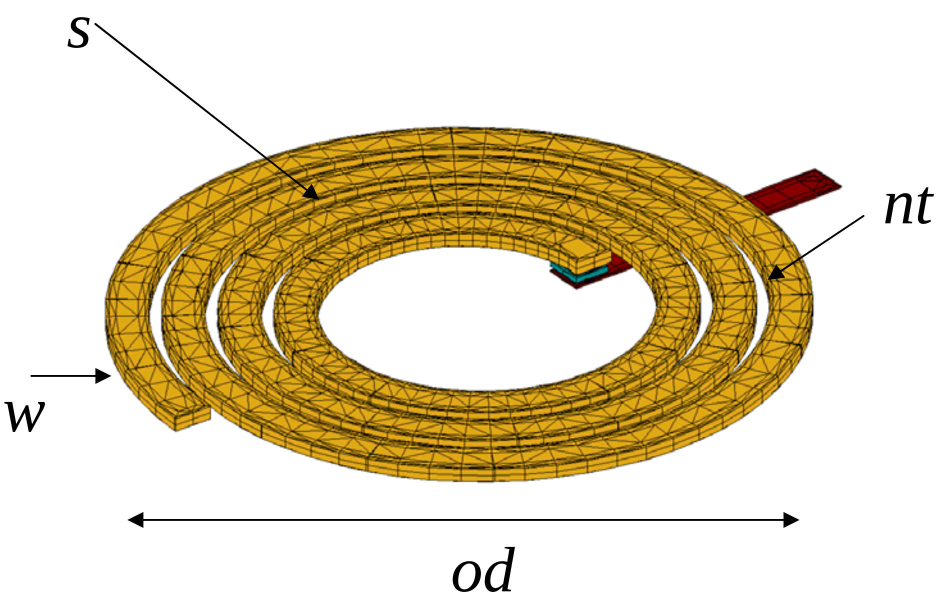


s=1.5um, nt=3.5

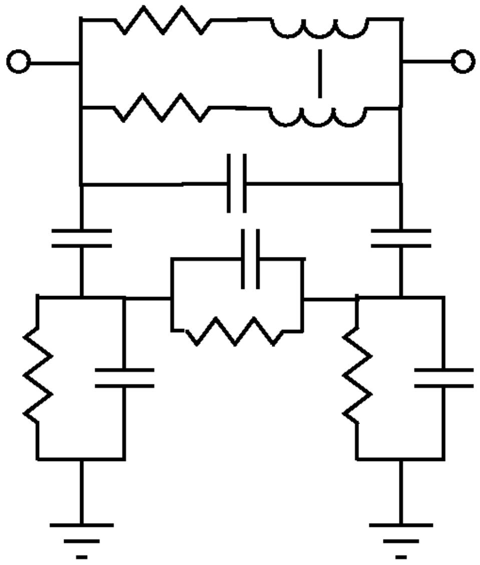
2D Projection

- Intuition
  - For all passive structures
  - Small changes in geometry
    - result in *small* “smooth” changes in electrical characteristics
    - L, Q

Parameterized Model



Inductor Model



$$Lc = f1(w, od, nt, s)$$

$$Csub1 = f2(w, od, nt, s)$$

$$Rsub2 = f3(w, od, nt, s)$$

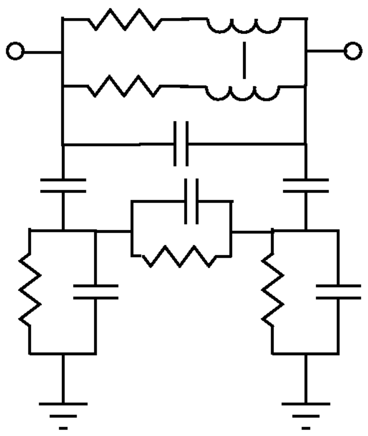
...

...

Every component in subcircuit is accurately captured by a function that is parameterized by geometry

Scalable Model vs Table Lookup

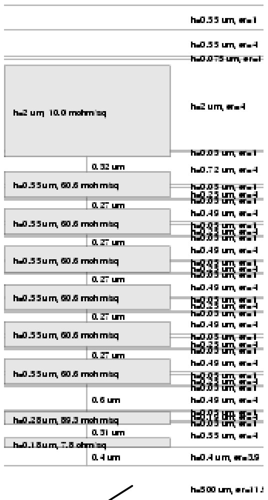
- RLCK model has several advantages
  - Compact representation
  - Portable across Spice simulators
    - Spectre, ADS, Eldo, HSPICE
  - Noise analysis and transient behavior correct
- Table lookups are always “clunky”
  - Discontinuous
  - Non-portable
- Spice models are C^{∞}
  - usable in a gradient-based design space search
- Main difficulty is automatically building the spice representation



EMX-Continuum™

- Scalable Model Generator
  - Discretization of space
  - Built from 1000s of individual inductor simulations
  - EMX as simulation engine
  - Proprietary techniques used to develop “unified” model
  - Accurate to few percent for L and Q compared to EMX simulation (user specified tolerance)
  - Pure RLCK Spice
  - Passive by construction
  - Noise analysis correct

Design Space
nt: 1.5 to 7.5 turns
W: 3um to 10um
S: 1.5um to 5um
OD: 75um to 300um



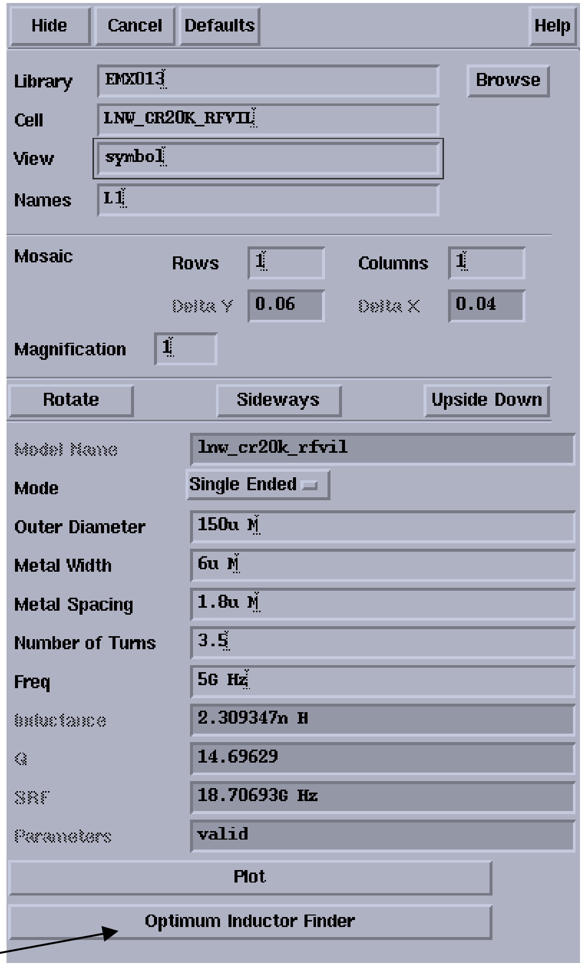
Layout generator
(UMC Cadence PCELL)

EMX-Continuum

Spice Models
Spectre, Eldo, Hspice, ADS

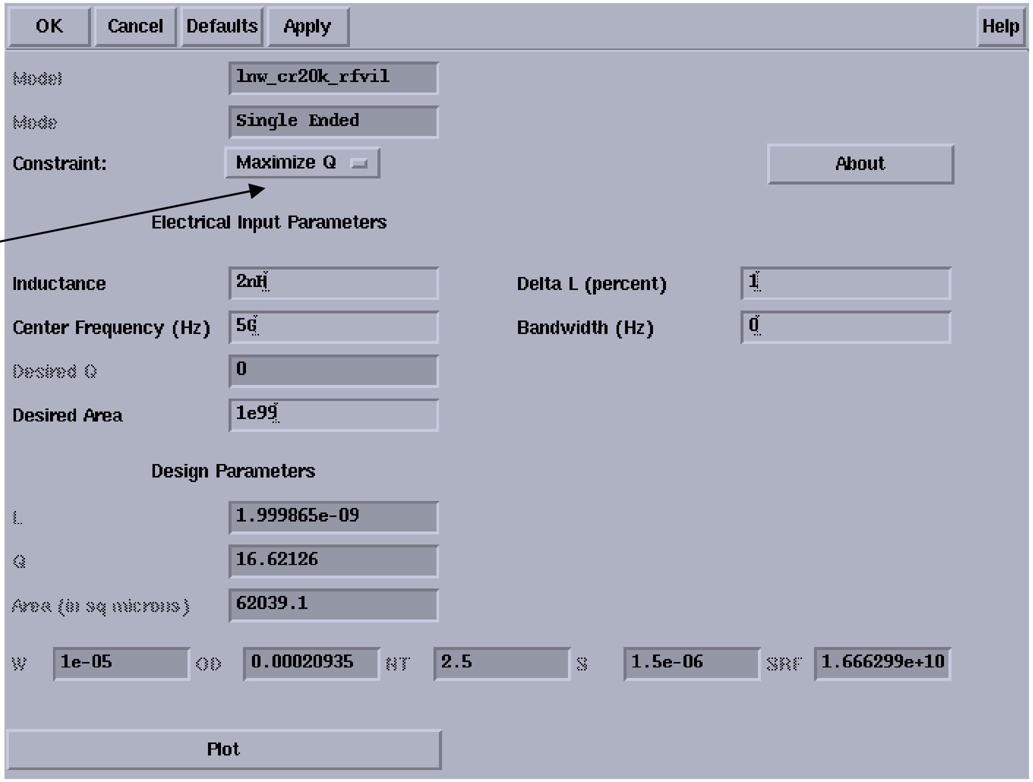
The Optimum Inductor Finder

- Design Space Prober
  - Finding optimal inductor design
  - Using the scalable spice models
  - Gradient-based approach for finding designs in high-dimensions
  - Accurate within a few percent of EMX
  - Almost instantaneous playback (5-10s)
  - GUI interface in Cadence Virtuoso
    - *Enabled by Integrand's membership in the Cadence Connections Program*
  - Integrated with UMC FDK
  - Can make Area/Q/Bandwidth tradeoffs for optimal design synthesis



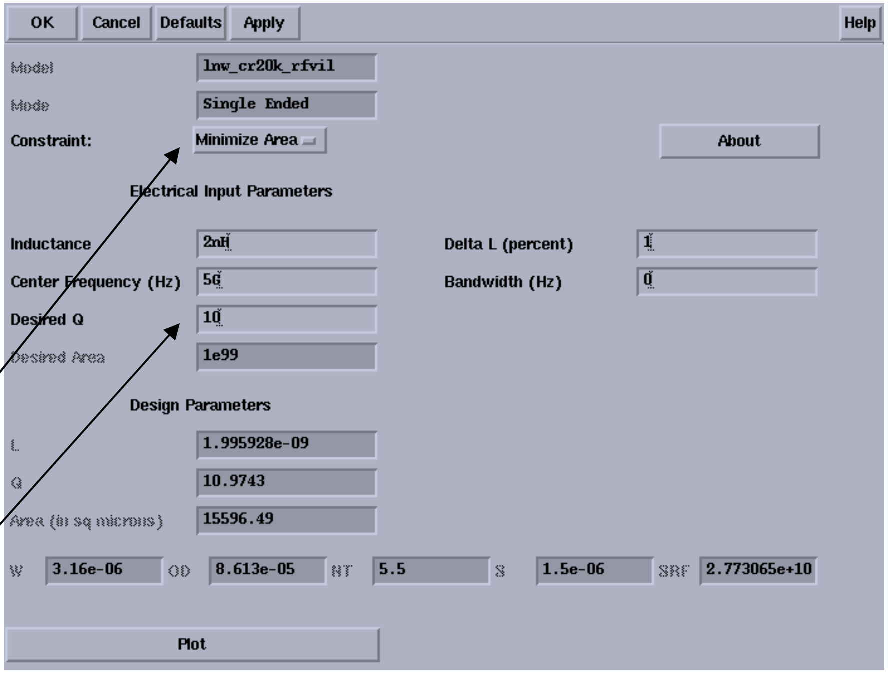
Maximize Q

- Maximizing Q is one of the most important metrics of inductor design
- Given inductance
- Find the inductor
  - With best Q
  - No constraint on area
- About 5s run time

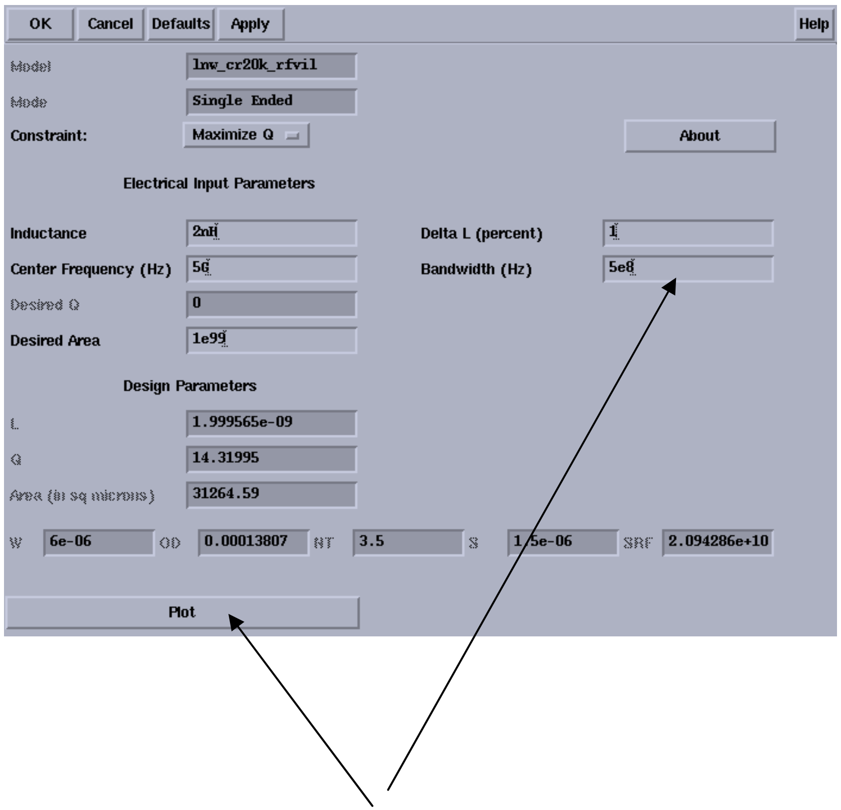


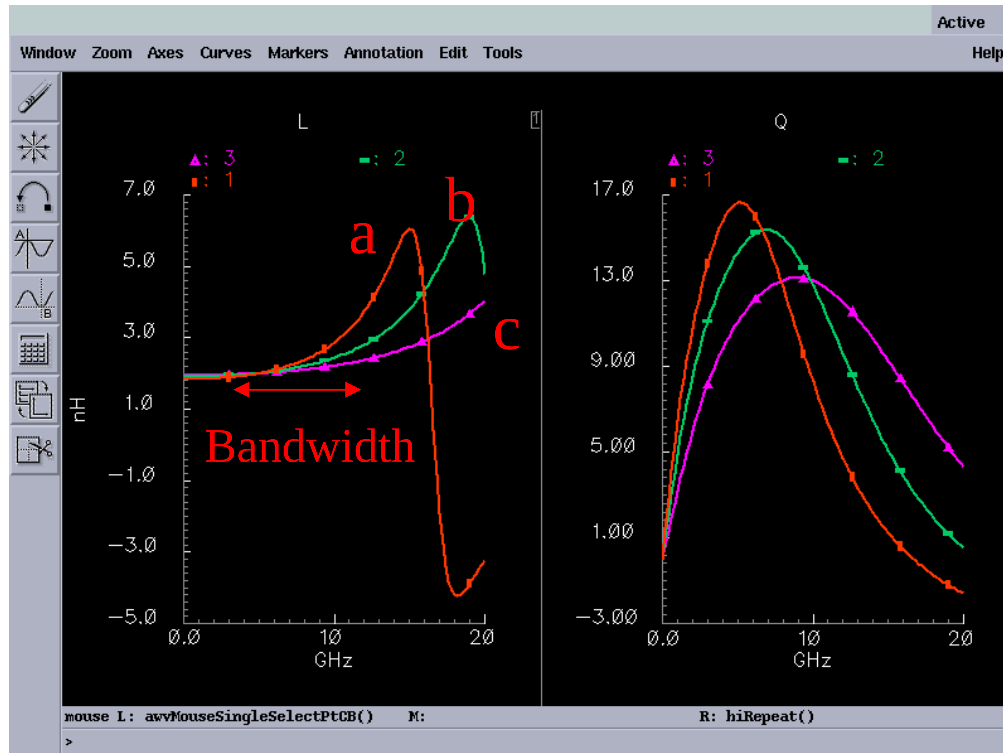
Minimize Area

- 50% of the area on a typical RF chip is consumed by inductors due to large area requirement
- Can find inductors with slightly less Q but much less area
- Given Inductance
- Find the inductor
  - With at least user-specified Q
  - With minimum area



Optimal Inductor Design for UWB

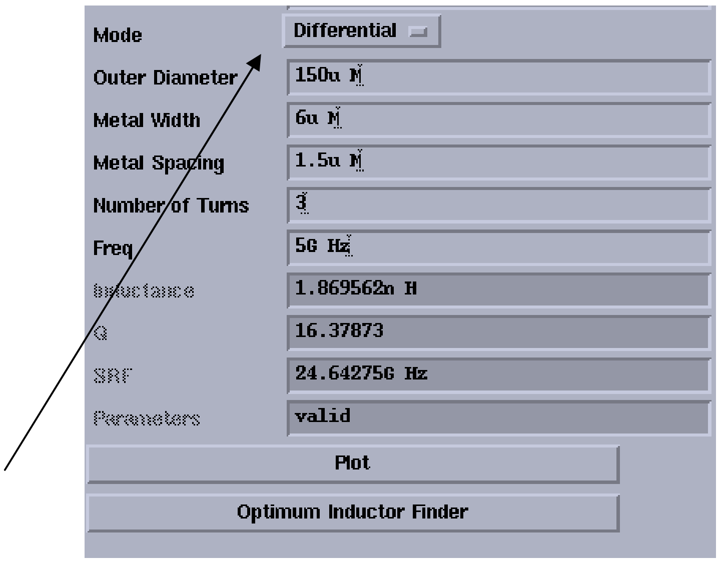




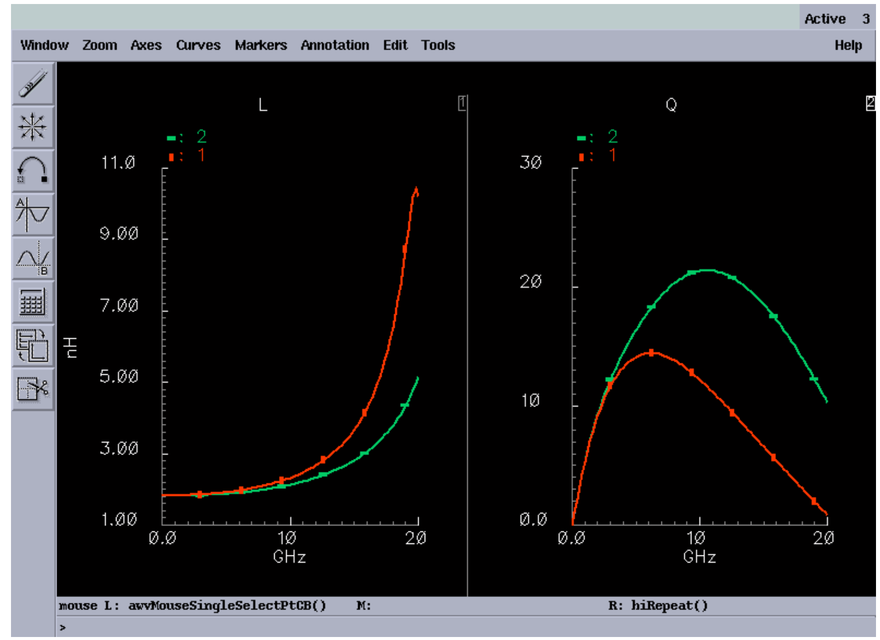
Trading Q for consistent inductance over wide bandwidth

The goal of UWB design is to “flatten the inductance”

Differential Design



- Differential model operation to reduce capacitive substrate loss



Single Ended vs Differential Inductor

UMC's FDK with the Optimum Inductor Finder

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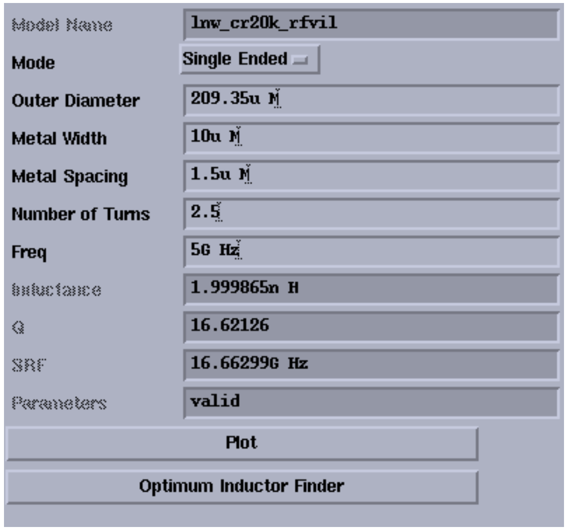
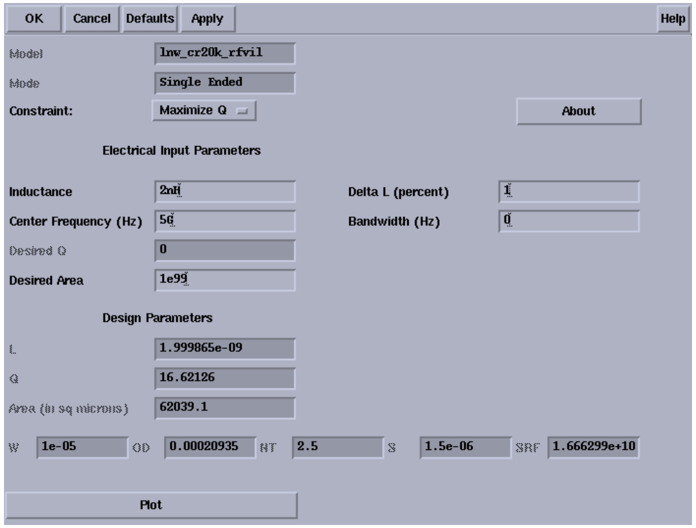
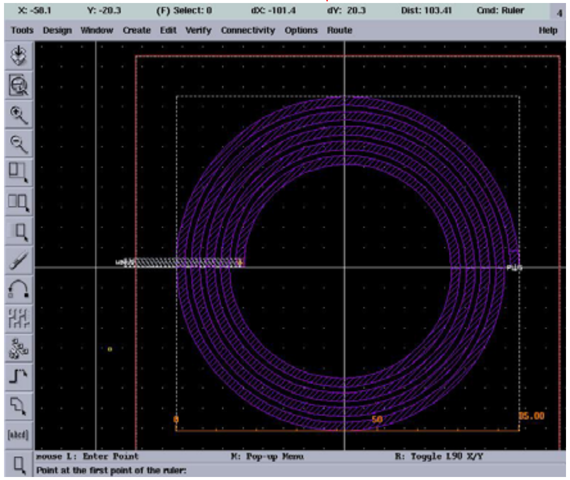


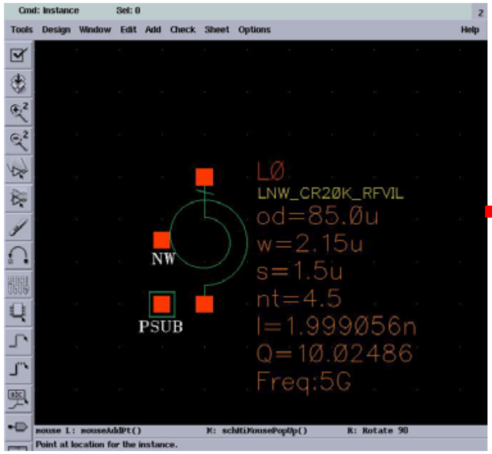
CDF



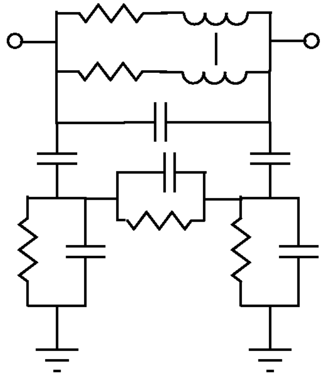
OIF



Layout View



Symbol View



Scalable Spice Model

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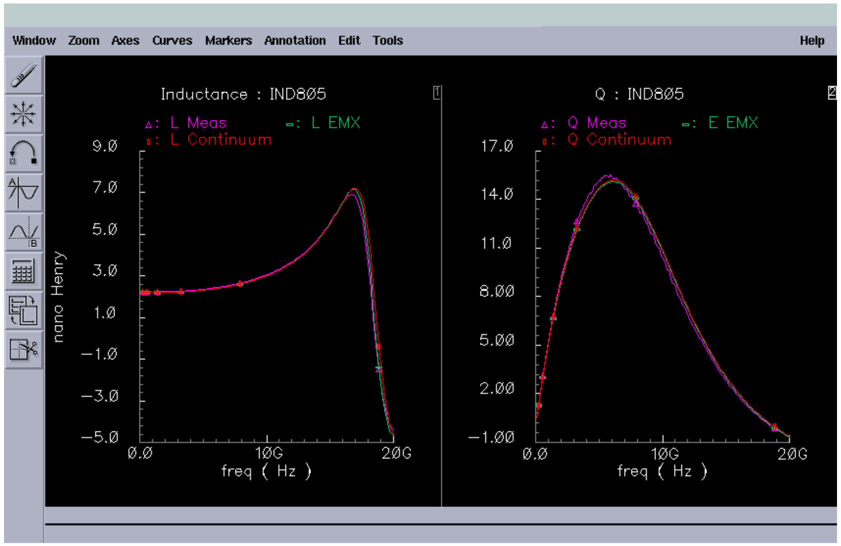
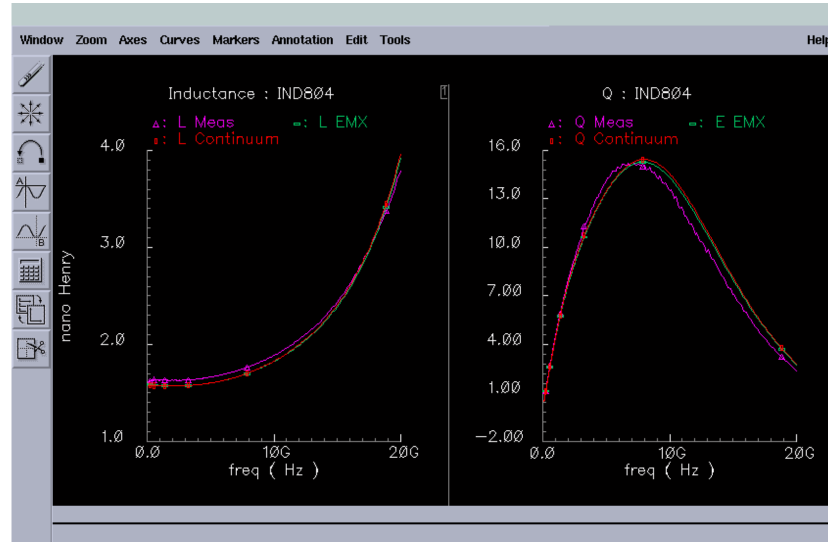
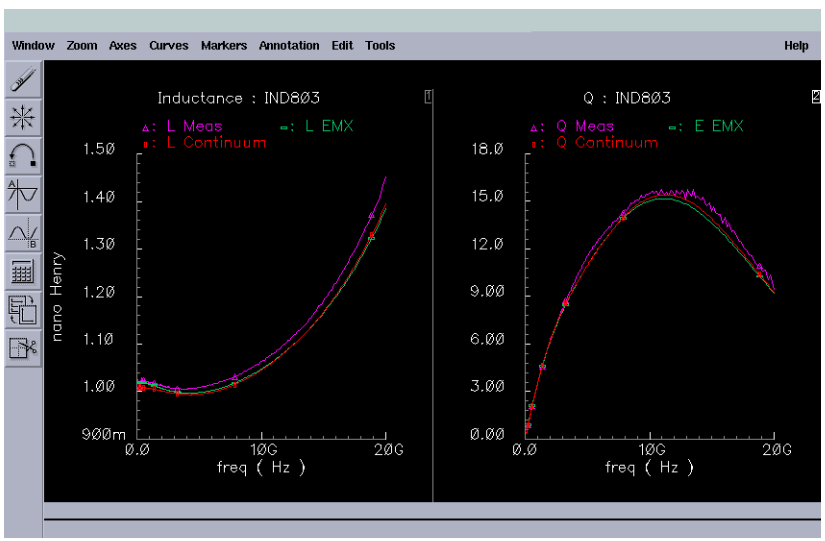
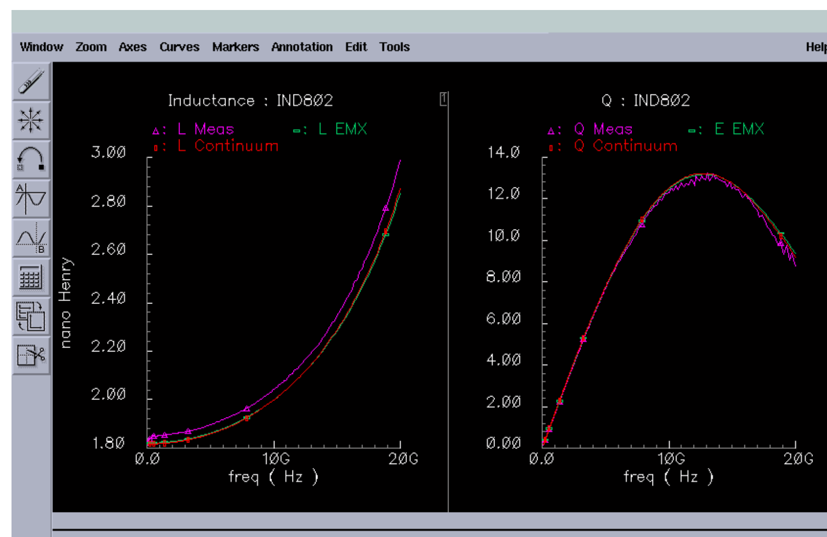
Typical Model Accuracy









Conclusion

- UMC Research and Development Team
  - DS: Tsun-Lai Hsu, Tony CP Liao, Liwei Lin, Jeff Liu
  - CRD: Yu-Chia Chen, Bigchoug Hung, Alfred H.C. Tseng, Victor Liang
  - UMC-USA: Zheng Zeng, Jin Shyong Jan, L.C. Yeh
- Successful and ongoing collaboration between UMC and Integrand Software Inc.
  - Extend the functionality of the UMC FDK to develop scalable models for other passives