A 3.1-9.5 GHz Agile UWB Pulse Radio Receiver with Discrete-Time Wideband-IF Correlation in 90nm CMOS

Frank Zhang†, Ranjit Gharpurey‡ and Peter Kinget†
† Columbia University, New York, NY 10027 USA
‡ University of Texas, Austin, Texas 78712 USA

***Abstract*— An 8-channel 3.1-9.5 GHz UWB pulse radio receiver is realized using a double-conversion architecture with discrete-time wideband IF correlation. The pulse templates for correlation are pre-stored in memories which allows fast band switching and agile interferer avoidance since no PLL resettling is required. The receiver chip is implemented in a standard 90 nm CMOS process and occupies 1 mm^2.**

I. Introduction

Ultra-wideband (UWB) systems must coexist in the 3.1-10.6 GHz band with a variety of primary, higher power wireless applications, making them susceptible to narrowband interferers. This work addresses the interference challenge at the architectural level through a combination of interference detection with agile avoidance, frequency planning and filtering. A 3.1-9.5 GHz double-conversion pulse radio receiver performs discrete-time wideband-IF correlation with pulse templates pre-stored in 2.11 GHz high speed memories. Switching between bands only requires the switch between two fixed LO frequencies for the first quadrature wideband downconversion and/or an update of the pulse shape in the digital memories. The developed frequency plan allows the generation of all on-chip LO frequencies and clocks from a single RF reference in a fixed divider chain. No PLL resettling is required to achieve band switching.

II. Frequency Plan

Fig. 1 shows the frequency plan of the receiver: the 3.1-10.6 GHz band is divided into 500 MHz-wide channels to reduce the sensitivity of the pulses to group delay distortions and to alleviate synchronization requirements at the receiver. This frequency plan allows for 14 channels, of which Channels 1-8 are covered by the receiver prototype. To cover additional channels, e.g., Channels A-F, the IF sampling frequency must be increased from 2.11 GHz to 4.22 GHz (discussed in more detail later).

The proposed pulse radio system uses an interferer detector (see [1], not implemented on this chip) to quickly scan through the spectrum and determine which channel has the least interferer power and therefore is most suited for communication. The block of channels around $LO1_{LB}$ or $LO1_{HB}$ is first downconverted to DC based on the selected band. The folding of the spectrum around the LO1s pushes the most important existing 802.11 interferers at 2.4 GHz and 5.25 GHz to higher IF frequencies where they are attenuated by lowpass filtering at the mixer outputs. The downconverted IF-pulses are then correlated with digital templates stored in receiver

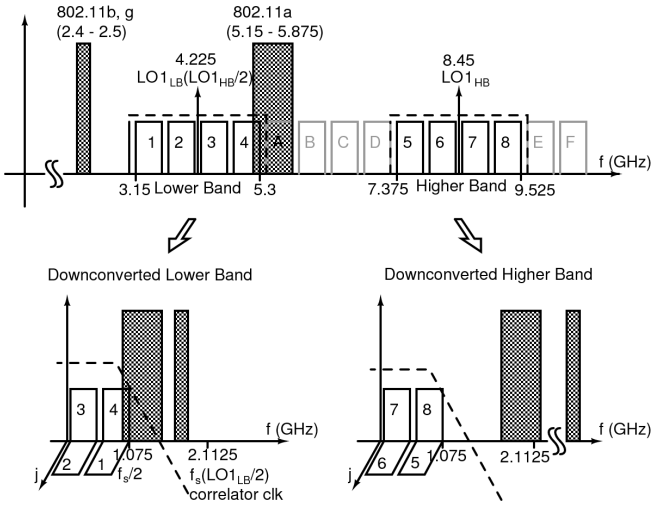

Fig. 1. Frequency plan of the pulse radio receiver before and after the first wideband downconversion, shown with existing 802.11 WLAN interferers.

memories; within a band, the upper sideband channels are distinguished from lower sideband channels through complex signal processing in the receiver architecture [2].

III. UWB Correlation Receiver

Fig. 2 shows the block diagram of the receiver; the signal is first amplified through a single-ended 3-stage distributed LNA (a detailed schematic is shown in Fig. 3) that provides true broadband gain and impedance matching in the 3-10 GHz range. Bondwire inductance and pad capacitance have been integrated into the distributed design to allow the circuit to function in a packaged environment. The die is placed off-centered in the 64-pin QFN package to minimize the length of the bondwires shown in the schematic. The ground bondwire inductance degenerates the LNA gain and degrades the input impedance matching of the amplifier and therefore must be minimized. Four bondpads are reserved for LNA GND, which are directly downbonded to the paddle of the package. The characteristic impedance of the drain line had to be kept low (75 Ω) to maintain the large bandwidth in the system but this limits the achievable gain. This design tradeoff between bandwidth and power/noise is repeated through out the receiver frontend to achieve close to full UWB band operation without external tuning. The LNA has a simulated voltage gain of 12 ± 1 dB and NF of 2-4 dB over the passband. The LNA is followed by two single-balanced active switching mixers driven by differential quadrature LO sig-

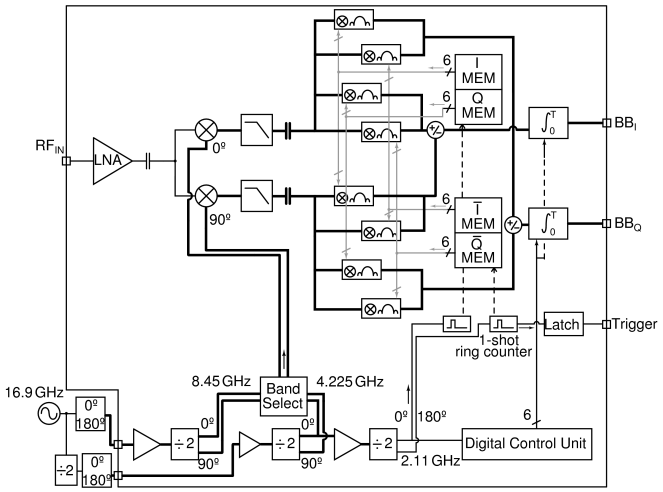

Fig. 2. Block diagram of the double-conversion receiver with digital IF correlators (thick lines indicate differential signal paths).

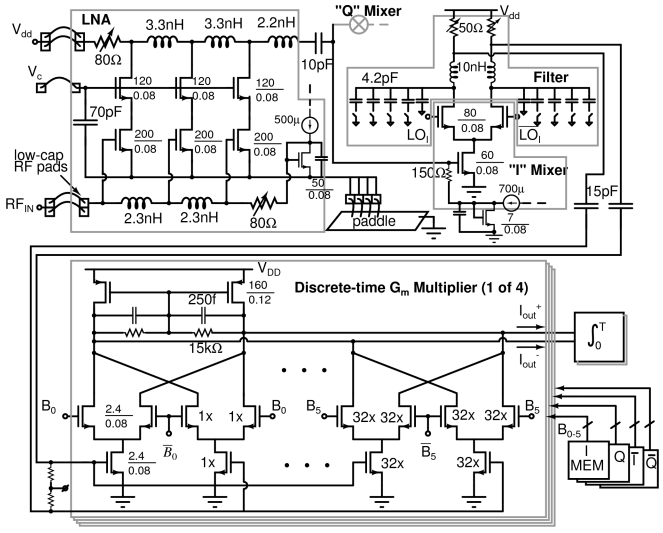

Fig. 3. Schematics of the LNA, mixer, filter and $\mathrm{G_m}$-multiplier.

nals with frequency selectable between 4.225 and 8.45 GHz. Single-balanced mixer provides single-ended to differential conversion without additional capacitive loading on the LNA, which would not only limit the signal bandwidth, but also adds excessive phase to its drain line. The load of each mixer is an on-chip 3^{rd}-order LC lowpass/anti-aliasing filter with a nominal bandwidth of 1.075 GHz which attenuates the mixer LO feedthrough as well as the interferers. The filter is a singly-terminated Butterworth minimum-inductance pi-network with transfer function: $\mathrm{Z_{21}(s)} = \frac{\mathrm{K}}{\mathrm{s^3+2s^2+2s+1}}$ [3]. After frequency transformation and translation on the prototype filter, the values of filter components are shown in Fig. 3. The input capacitance of the 6-bit correlators following the mixers is ~ 1.5 pF and forms the second capacitor of the filter. To achieve a fixed filter Q, the value of the load resistor and the inductor cannot be be chosen independently. The inductance value is limited by available chip area, which limits the maximum value of the load resistance, which in turn limits the gain of the mixer. The 10 nH inductor used in the filter consists of a spiral designed in $\mathrm{MT9}$, in series with a second spiral made of $\mathrm{MT8}$ and $\mathrm{MT7}$ in parallel, laid out underneath the first spiral to limited its area to 170×170 μm^2. A bank of binary-weighted capacitors with a nominal value of 4.2 pF is used for tuning to compensate for device variations. The simulated voltage conversion gain of the combined mixer-filter is 0 dB for Lower Band and -4 dB for the Higher Band; the out-of-band attenuation of the filter is ~ 14 dB/octave.

A wideband discrete-time complex correlator is implemented at the IF frequency. The use of complex correlation significantly reduces the synchronization requirements on the receiver since the proper combination of the I and Q paths eliminates the sensitivity to the RF carrier phase for AM pulse formats or differential PM pulse formats. The correlators are implemented with 6-bit binary-weighted discrete-time $\mathrm{G_m}$-multipliers; pseudo-differential pairs are used as transconductors to reduce headroom requirement and to provide adequate linearity given the 1.2 V supply. The digital data used to switch the $\mathrm{G_m}$ elements comes from fast memory blocks which store the quadrature pulse templates. The outputs of the $\mathrm{G_m}$-multipliers are currents proportional to the product of the downconverted received signal and the digital representation of the IF pulses. This receiver prototype has one set of memories, while adding a second set will allow pulse to pulse channel hopping since the two sets can work in an alternating fashion between preloading and correlating. The clock used to output the digital data is 2.11 GHz, which is half of $\mathrm{LO1_{LB}}$ and twice the frequency of the cutoff frequency of the anti-aliasing filter. The multipliers are interleaved to increase their effective sampling frequency to 4.22 GHz, thus pushing the IF sampling images from the 1-2 GHz range to the 3-4 GHz range where the lowpass filter has higher attenuation. The currents from the four complex signal paths are added or subtracted to select the channels from the lower or upper sideband respectively. As shown at the bottom of Fig. 2, all the clocks used in this receiver can be generated from a single external source through current-mode logic (CML) dividers; in the actual implementation, a second redundant divider chain is added for testability. In a single chip transceiver implementation these clocks can be shared with the interference detector and the transmitter.

The combined $\mathrm{G_m}$-multiplier outputs are integrated with a switched-capacitor (SC) integrator shown in Fig. 4. In the integration mode, ϕ_{A}, ϕ_{B} are the same and the currents from the multipliers are integrated on to capacitors $\mathrm{C_A}$ and $\mathrm{C_B}$ and the charge is transferred to $\mathrm{C_3}$ during ϕ_{ADD}. The SC integrators have the option for a synchronization mode where ϕ_{A} and ϕ_{B} are non-overlapping and the current is integrated for half of a period on $\mathrm{C_A}$ and another on $\mathrm{C_B}$, which can then be sensed through auxiliary circuitry and used for symbol synchronization. Two sets of SC circuits work in a rotating fashion such that when one set is charging the other set is transferring the charge to the output, similar to [4]. This maximizes the output symbol rate and relaxes the gain-bandwidth requirement on the OTAs. The 20-deep

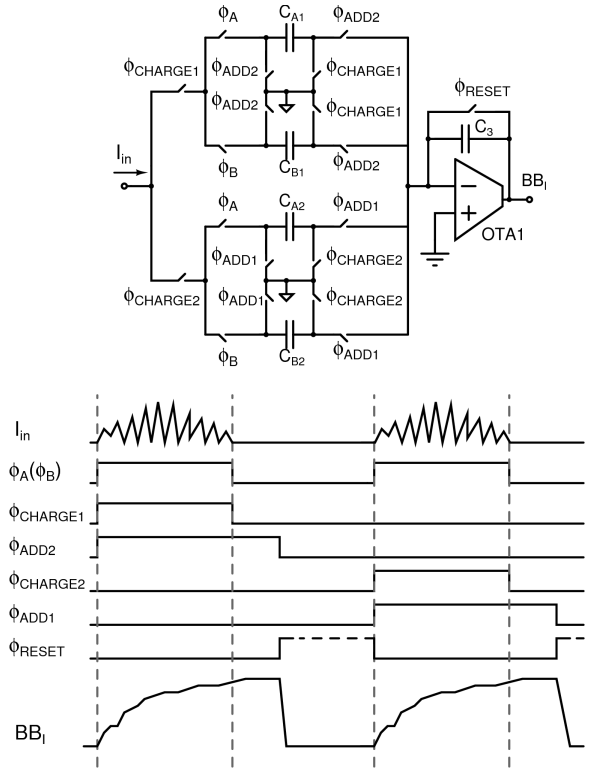

Fig. 4. Single-ended equivalent schematic of the rotating switched-capacitor windowed integrator and its timing diagram.

memory depth corresponds to a maximum symbol rate of 105.6 Msymbols/s. The bandwidth of the pulse as well as pulse-shaping is adjustable by changing the 6-bit wide data in the memories.

IV. Results and Discussion

Fig. 5 shows the measured output of the receiver for 8 different channel settings when the input is a sinusoid swept across frequency in steps of 10 MHz; the corresponding channel template for the pulse with time-limited, sinc-shaped envelope were used in the receiver, which minimizes the spectral leakage. The lower band channels and upper band channels were swept separately across a 3.5 GHz range in order to capture both the signal and the image bands. Each point on the plot is extracted from the quadrature outputs captured on a digital oscilloscope. The image rejection ranges from 12 dB to 21 dB, channels closer to their image channel have lesser rejection. Dedicated high gain setting in the LNA and the G_m-multiplier are used for the 4 upper band channels to compensate for the high frequency roll-off of the mixer. The lower Q of the LC lowpass filter contributes to the magnitude reduction in channels farther from the LO carrier.

BER measurements for a UWB pulse receiver requires a customized setup that includes the generation of the UWB pulses and proper output data acquisition. Fig. 6 shows our testbench setup, it consists a FPGA board and two signal generators. DAC1 of the FPGA generates random pulse envelopes, which are lowpass filtered and then upconverted using a vector signal generator. Top of Fig. 7 shows the

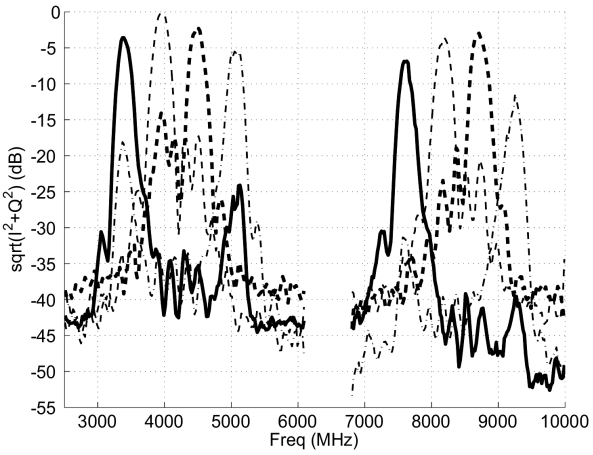

Fig. 5. Pulse receiver response to swept sinusoidal RF input when correlating with the corresponding template with time-limited sinc-shaped envelope for the 8 different channels.

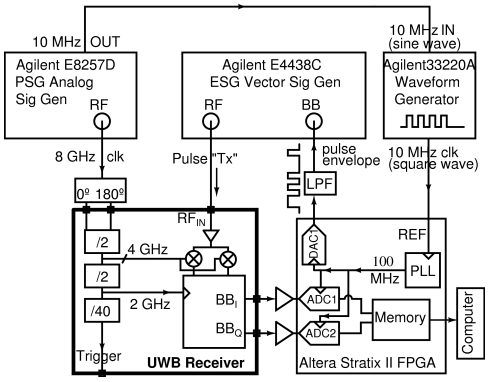

Fig. 6. UWB receiver BER measurement setup for 50 Mb/s OOK demodulation.

resulting UWB pulses, Pulse "Tx", with OOK modulation, as seen on a sampling oscilloscope. Due to baseband bandwidth limitations of the ESG generator, the shortest pulse envelope is 20 ns (50 Msymbols/s), therefore all frequencies in the measurement including the interferers are scaled by 100/105.6. However, the 20-deep memory depth of the receiver corresponds to a maximum pulse duration of 10 ns since the receiver was designed to correlate with pulses with much larger bandwidth. The limitation of the ESG generator forces each pulse to be correlated twice by the receiver, as shown by the quadrature outputs on the bottom of Fig. 7.

Synchronization in UWB systems is very challenging and is not the main focus of this work; for this measurement, only symbol synchronization is established between the "transmitter" and the receiver by locking the LO/clock generator of the receiver to the PLL of the FPGA through an external loop. Although OOK is used in the measurement, the availability of quadrature outputs also allows more complex modulation schemes such as DBPSK and DQPSK. Note in Fig. 7 that the $BB_I^2 + BB_Q^2$ pulses indeed detect the input bits, whereas I and Q outputs alone vary rapidly with the carrier phase. Two ADCs on the FPGA board sample the quadrature baseband outputs at 100 MS/s which are then processed off-line. Fig. 8 shows the

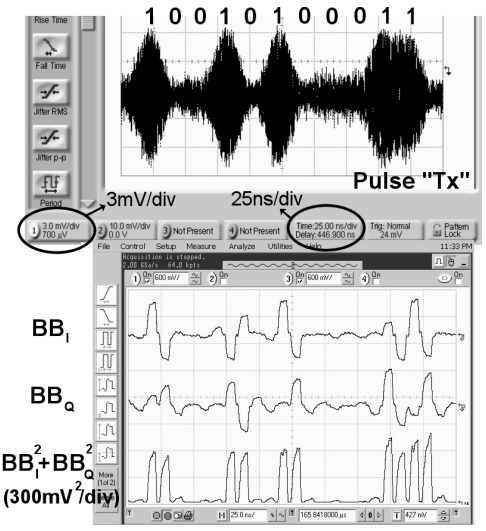

Fig. 7. Input UWB pulses and quadrature receiver outputs demodulating an OOK signal at 50 Mb/s; each input pulse is correlated twice and therefore produces two identical outputs for each bit (see text).

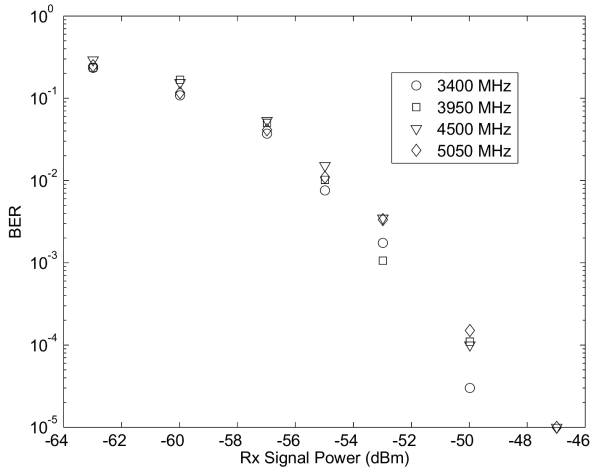

Fig. 8. Measured BER versus receiver signal power at 50 Mb/s using OOK modulation for different channels.

measured BER versus Rx signal power for the 4 Lower Band channels; BER for the Higher Band channels could not be tested due to the limited frequency range of the ESG generator. For Channel 2, the BER degrades from 10^{-5} to 10^{-3} in the presence of a 2.4 GHz interferer as large as -11 dBm or a 5.25 GHz interferer as large as -16 dBm. For Channel 1, the same degradation occurs for -13 dBm 2.4 GHz interferer and -21 dBm 5.25 GHz interferer. The receiver consumes 130 mA from a 1.2 V supply; the chip micrograph is shown in Fig. 9.

Table I compares the performance of this UWB receiver with previously published pulse radio receivers. This high data-rate receiver covers both the lower and higher bands of the UWB spectrum and avoids the use of tunable bandpass filters [5] that require manual adjustments for each channel and occupy a large area. The area of our receiver is small thanks to the extensive use of high-speed digital circuitry and memories that will scale in size and performance as technology improves.

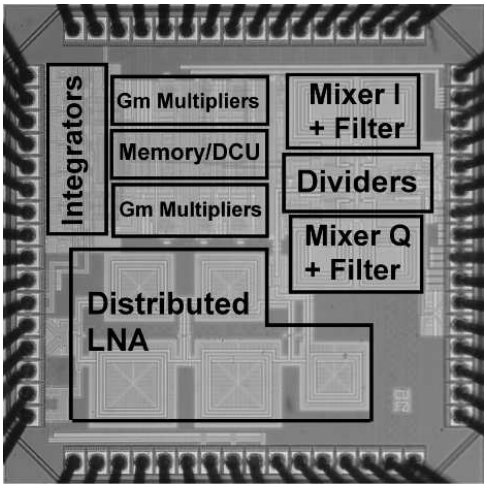

Fig. 9. Chip micrograph.

TABLE I
PULSE RADIO PERFORMANCE COMPARISON

	This Work	[6]	[5]	[7]
CMOS Tech.	90 nm	0.18 μm	90 nm	0.18 μm
Frequency	3.1-9.5 GHz	3-9 GHz	3-5 GHz	3-5 GHz
Sensitivity for 10^{-3} BER	-53 dBm @50 Mb/s	N/A	N/A	N/A
	-80 dBm @100 kb/s[1]	N/A	-99 dBm @100kb/s	N/A
Interferer Pwr to reduce BER from 10^{-5} to 10^{-3}	-11 dBm 2.4 GHz Int	N/A	-20 dBm 2.4 GHz Int	N/A
	-16 dBm Int 5.25 GHz	N/A	-15 dBm 5.25 GHz Int	N/A
Power	156 mW	137 mW	36 mW	29 mW
Modulation	OOK[2]	DSSS	PPM	PPM
Size	1 mm^2	4.8 mm^2[3]	2.2 mm^2	8 mm^2

[1] Subtracting 10log10(50M/100k) from measured sensitivity at 50 Mb/s.
[2] Measured; quadrature outputs also allow differential phase modulations.
[3] Part of a transceiver; receiver size estimated from die photo.

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