2.6-GHz RF Inductive Power Delivery for Contactless On-Wafer Characterization

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ABSTRACT

This paper presents the critical components of a contactless IC testing infrastructure to power on-chip characterization circuits. This includes an inductively-coupled, contactless power delivery system implemented on a 90nm CMOS technology using 150µm x 150µm on-chip and off-chip spiral inductors, low loss rectifiers and on-chip voltage regulators to create a constant and repeatable 1-V, 8.5-mW DC source. We present the measured process variation of ring oscillator test circuits in contrast to the on-chip voltage source variation to demonstrate the feasibility of process variation analysis using this system.

INTRODUCTION

A number of contactless testing solutions have been recently presented in literature utilizing different coupling mediums, such as RF coupling through micro-antenna structures [1,2] and optical coupling through CMOS photo-detectors [3,4]. The aim of a contactless approach is to provide access to on-wafer test structures in the early stages of the fabrication cycle, without damage to the wafer and without the need for ESD circuits. The delivery of DC power to the test structure is the most significant challenge in developing a contactless testing macro.

Power delivery though RF micro antennas, when realistically sized, is difficult due to low levels of coupling, thus requiring traditional mechanical probing connections to inject DC power when RF coupled power is insufficient [1], or alternatively, large on-chip antenna devices [2]. Optical coupling techniques have shown considerable promise in power delivery with small die space requirements [4], but require the design and characterization of specialized photodiodes typically not readily available in standard CMOS technologies.

The magnetic coupling of an off-chip spiral inductor positioned above an on-chip spiral inductor can achieve relatively high levels of coupling, enabling efficient contactless power delivery. At GHz frequencies the size of the spirals can be made comparable to traditional pad structures and the associated ESD circuits in standard CMOS technologies. Furthermore, the architecture and results presented here demonstrate that precise voltage rectification and regulation can be realized on-chip to present an accurate DC power supply. The generation of a repeatable, accurate DC power supply is the most important challenge in demonstrating a feasible contactless testing system, and is the focus of this paper.

SYSTEM ARCHITECTURE

To demonstrate a proof of principle, a compact and robust architecture was chosen as illustrated in Fig. 1; the on-chip power delivery macro consists of a spiral inductor, a CMOS rectifier, a linear regulator with OTA and power transistor, and a CMOS voltage reference; a ring oscillator serves as the device under test and load circuit; for testing an off-chip spiral inductor mounted on a micro-positioner is placed over the macro and driven by a standard RF signal source.

The inductors were simulated with an EM simulator, EMX, to obtain broadband frequency domain s-parameter data. An equivalent circuit, as shown in Fig. 2, was extracted using Matlab optimization routines. Since changes to the transformer's physical structure result in direct changes to the values of the lumped circuit elements, this design flow makes circuit optimization more intuitive. For instance; the

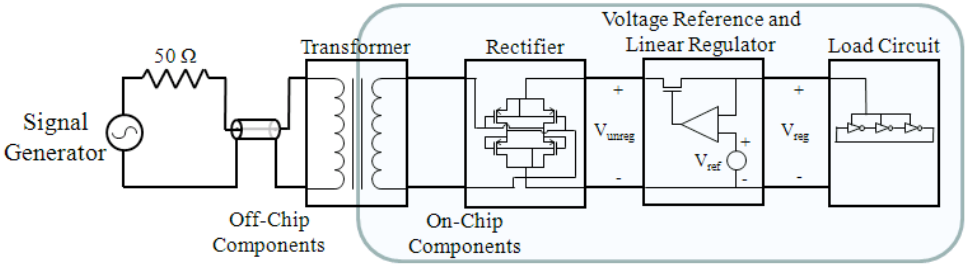

Fig. 1. Diagram of the Proposed Contactless IC Testing Architecture

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numerous degrees of freedom in transformer topology can be optimized to find a structure with desirable low series resistances and high coupling coefficient at a given frequency, even though important second order effects make precise hand calculations too difficult. The dimensions of the inductor were then optimized for maximum power transfer efficiency (PTE) through circuit simulation of the equivalent transformer circuit in combination with the RF rectifier (described later). We obtained the best PTE with a 3-turn 150µm x 150µm off-chip inductor and a 5-turn 150µm x 150µm on-chip inductor realized in the top metal layer. Minimum metal spacing of the spiral traces was used to result in desirable high Q and low loss inductors. The spacing between the on-chip and off-chip inductor was assumed to be less than 50µm.

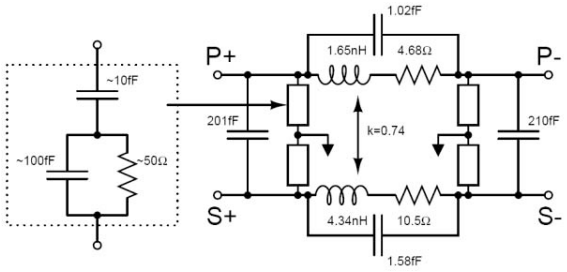

Fig. 2. Transformer Equivalent Circuit Model.

On-chip ring oscillators are commonly used to characterize device performance and process variation across and between wafers. We used a digitally programmable, variable load, 57-stage ring oscillator as a circuit under test to load the power delivery macro.

The RF rectifier block, shown in Fig. 3, uses a combination of low threshold MOS diodes (M3 and M4) and low threshold pass-transistors (M1 and M2) to implement efficient full-wave rectification of the RF signal in the used 90nm CMOS technology. PMOS devices were used to increase isolation from the substrate and careful consideration was given to the resonance conditions between the transformer structure and large rectifier capacitances. To tune the rectifier input impedance and to decrease effective series resistance, multiple copies of the rectifier structure were connected in parallel to decrease current density and thus series voltage drop. For RF frequencies, a combination of pass transistors and diode devices provides a reasonable tradeoff between low series resistance (typical of diode rectifiers) and low V_T drop (typical of pass transistor rectifies). Rectifier topologies based on pass transistors only were not feasible at RF since they require special gate drivers to prevent shoot through currents and the associated power losses.

A compact on-chip linear regulator was used to ensure robustness and simplicity, where the OTA is a single stage design biased in weak-inversion to minimize power consumption. A low power, on-chip bandgap reference based on [5], was designed for use in this project.

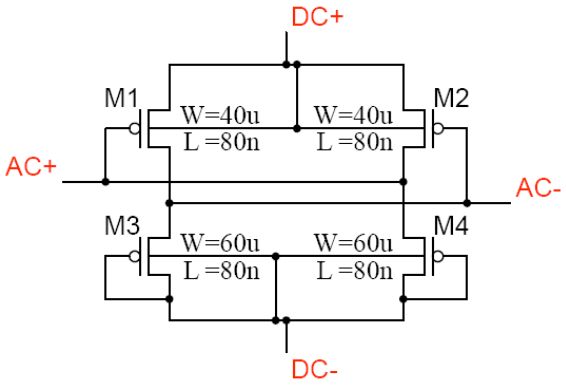

Fig. 3. 2.6GHz RF Rectifier Schematic.

IC IMPLEMENTATION

The designs were fabricated in a standard 90nm CMOS technology and tested for functionality. Fig. 4 shows the die photograph and the layout of the power delivery macros and the ring oscillators serving as circuit under test. Note that the power supply circuitry is of comparable size as the 150µm x 150µm inductor devices. For future designs these devices could be placed inside or underneath the inductors further reducing die space using the design techniques demonstrated in [6]. Alternatively they can be placed in space reserved for wafer dicing to preserve metal layer resources near the DUT. To test circuits early on in the fabrication cycle, layouts using only one layer of metal can be considered for future designs.

To verify this proof-of-principle design we added the top and bottom DC bondpads to observe internal DC voltages and digitally control the ring oscillator load during testing, while the left hand side bondpads are for RF output. Ultimately no DC bondpads will be needed and the RF output can be coupled back through the transformer; also, control signals can be modulated on the RF input signal as is standard practice in other inductive link designs [8,9].

The system is duplicated into two separate test cases; the *spiral only test case* and the *transformer test case*. In the *spiral only test case* the primary inductor of the transformer is to be fabricated on an external substrate. The secondary inductor is realized on chip in the top metal layer. The proper functionality of the *spiral only test case* is the ultimate goal of this project. Also available is an output buffer and output probing pads to bring the ring oscillator output signal to a spectrum analyzer for the measurements of the ring oscillator process variation.

In the *transformer test case* the secondary inductor is realized on-chip in the top two metal layers while the primary is laid out in the two metal layers below such that the entirety of the transformer is on-chip. The purpose of this case was to demonstrate system functionality without the need of fabricating external

probing inductors. The ring oscillator output signal is not externally available for this case.

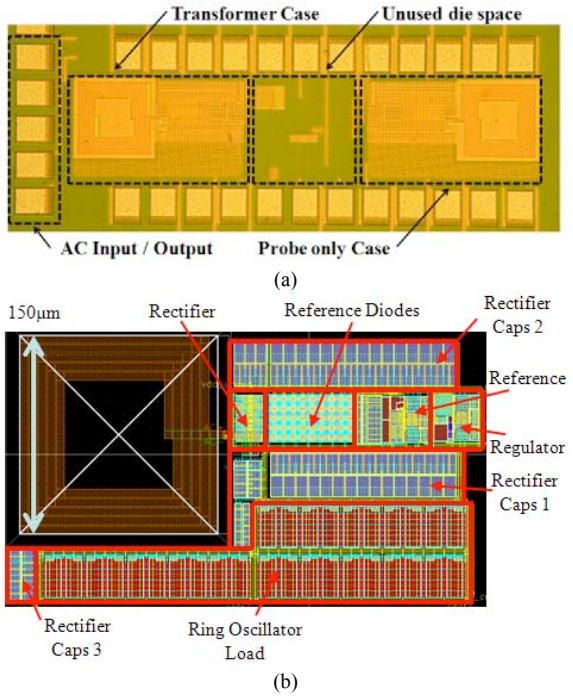

Fig. 4. (a) Die Photograph; (b) Layout of Probe Only Test Case.

As of the time of this writing, prototypes for the external thin film, probing inductors to test the *spiral only test case* are being fabricated with photolithography in our in-house clean room facilities. This process includes chrome-gold spirals, with polyimide insulator deposited on thin glass substrates. These devices are to be mounted on PCBs and placed in close proximity to the surface of the DUT using micro-positioners. However, due to photolithography complications, the fabrication process details are not yet finalized and the testing results using this system will be presented in a future work.

To still demonstrate external magnetic coupling, but without fully optimized external probing inductors, an external probe inductor structure was manufactured on a PCB. However, only a single turn, 127µm inductor device with transmission line feed and matching circuitry could be fabricated due to the layout constraints on a standard 5mil PCB process. Such inductor geometry leads to substantially poorer coupling as with optimized thin-film probing inductors, given that the magnetic field strength from a low turn device is significantly reduced.

MEASUREMENTS AND RESULTS

In a first set of tests we measured the *transformer test case* to demonstrate the feasibility of reliably delivering DC power to a test circuit using the presented test macro. In Fig. 5 a 16-dBm RF sinusoid[1] between 2.6GHz and 2.7GHz is delivered to the on-chip primary inductor. This results in sufficiently large *Vunreg* so that the on-chip regulator can provide a stable 1-V power supply to drive the ring-oscillator load which represents 8.51mW of loading. We have further measured that a 14-dBm RF signal to the transformer is sufficient to drive a 4.0mW ring-oscillator load. Additionally, we have found an excellent *Vreg* insensitivity to variations in loading conditions, RF input power, and RF input frequency. In Fig. 5, 100mV variations in *Vunreg* due to variations in received power as a result of changes in input frequency from the optimal 2.69GHz, result in less than 1mV changes to *Vreg*. Typically, we have measured 10mV/V sensitivity of *Vreg* to changes in *Vunreg* .

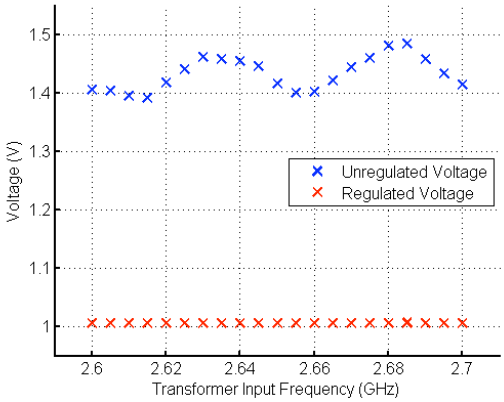

Fig. 5. Measured Regulated Voltage versus Input Frequency.

Fig. 6 illustrates the measured statistical distribution of the regulated and the unregulated voltages across 52 TT dies from the same wafer. A 13-dBm 2.69-GHz RF sinusoid was applied to the transformer test case with 4mW of DC loading. The average unregulated voltage was approx. 1.3V with a σ of 72.5mV, due to impedance mismatches, device variations, variable loading conditions and other effects. The regulated voltage had a mean of 1.0V with a σ of only 14.5mV. Additional tests with an input power at 12dBm and 11dBm which are below the nominal power of 13dBm are summarized in Table. 1. Note that an 11-dBm input power is marginally sufficient for the tested loading conditions and would not be used in practice.

[1] During our initial testing we had access to a 16dBm RF generator which became unavailable later; subsequent tests had to be done with maximum RF power of 13dBm.

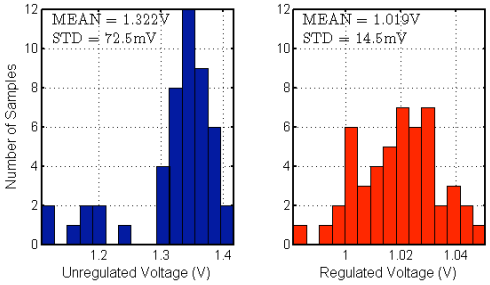

Fig. 6. Measured Statistical Distribution of Vunreg and Vreg across 52 samples.

Input Power (dBm)	$\mu(V_{unreg})$ (V)	$\sigma(V_{unreg})$ (mV)	$\mu(V_{reg})$ (V)	$\sigma(V_{reg})$ (mV)
11	0.970	31.4	0.954	30.6
12	1.111	58.3	1.010	18.5
13	1.322	72.5	1.019	14.5

Table 1. Measured Statistical Variation of Transformer Test Case *Voltages for Varying RF Input Power; 13dBm is the Nominal RF Input Power*

To demonstrate a practical application for this contactless power delivery macro, we investigated the possibility of monitoring the frequency variation of the 57-stage ring oscillator load during a second set of tests. Note that the ring oscillator inverter devices were sized with non-minimum length, and a large number of stages was chosen such that the frequency was approximately 500MHz; low enough to prevent coupling with the 2.69 GHz RF power carrier. However, larger device sizes and larger number of stages reduce the variability of the ring oscillator output frequency.

Fig. 7 illustrates the statistical variation of the 57-stage ring oscillator on the 52 dies tested, when the unregulated supply, V_{unreg}, of the probe only test case is driven by an external 1.35V DC power supply. An average frequency of 432.6MHz with a σ of 13.4MHz was found. The mean and sigma of the regulated supply voltage was also measured and found to be 1.019V and 14.5mV respectively. The supply pushing of the ring oscillator has been measured to be less than 510 MHz/V; the σ in the output frequency due to supply variations is then 7.4MHz which is significantly smaller than the total measured ring oscillator frequency σ. In addition, even when the unregulated voltage is significantly lower and higher than 1.35V nominal, the variation in regulated voltage in contrast to the variation in ring oscillator frequency is still statistically significant. A summary of these results is shown in Table 2.

As shown in [7], for future work it will be possible to design ring oscillators with fewer stages, followed by dividers, which will exhibit more pronounced frequency variations. Additionally designs highlighting different process variation effects can be used.

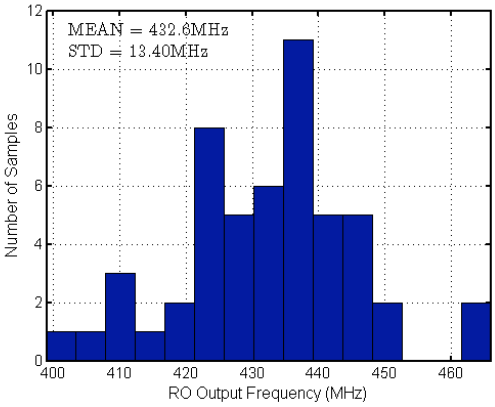

Fig. 7. Measured Statistical Distribution of the Ring Oscillator Frequency Across 52 Samples.

V_{unreg} (V)	$\mu(V_{reg})$ (V)	$\sigma(V_{reg})$ (mV)	μ(freq) (MHz)	σ(freq) ($MHz_)$
1.1	0.993	8.84	417.2	10.37
1.35	1.019	15.0	432.6	13.40
1.6	1.021	14.9	433.9	13.77

Table 2. Measured Statistical Variation of Probe Only Test Case *Regulated Voltage and Ring Oscillator Frequency.*

In a third set of tests we brought the single turn PCB inductor (described above) into close proximity to the on-chip inductor of the *spiral only test case.* Due to the low number of turns and large size of this inductor, it was only able to couple a small amount of power into the on-chip devices. We found that applying our maximum RF power of 13dBm to the probing inductor resulted in only 735mV unregulated voltage at the output of the on-chip rectifier. This is insufficient to adequately provide enough voltage for the regulator to output a regulated 1V V_{DD}. We anticipate far better results with thin-film external probing inductors which can be designed with the correct size and number of turns.

We used the PCB inductor to perform a preliminary evaluation of the probe misalignment on the system performance. As shown in Fig. 8, it was found that within +/- 50μm lateral misalignment from the optimal probe position, the unregulated voltage drop was no less than 350mV. Within +/- 5μm displacement, which is a reasonable alignment tolerance for most micro-positioner devices, an unregulated voltage drop of only 5mV was found suggesting good insensitivity to probe misalignment. Also note that our earlier test have demonstrated that the regulated output voltage is very accurate over a large range of unregulated voltage values which further adds to the system robustness.

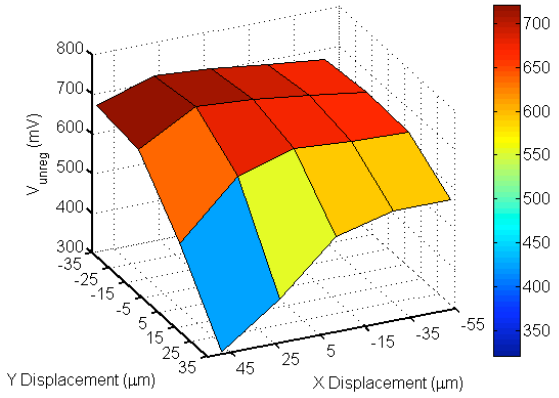

Fig. 8. Measured effect of PCB Probe Misalignment on Unregulated Voltage

SUMMARY

We present a system to power integrated test circuits without making physical contact for use in wafer characterization testing. The system is capable of supplying 8.5mW of regulated DC power from 16dBm AC power, to digital switching loads. The on-chip regulated 1V supply repeatability was shown to be sufficient for variation analysis of ring oscillators. Using an external PCB probe device promising insensitivity to lateral probe misalignment of less than 5mV drop within +/- 5µm was recorded.

Future extensions to this work will include supply macros capable of transferring digital data through modulation of the power carrier and the load impedance as has been shown feasible in literature [8,9], with minimum impact on power transfer efficiency. To save space, components can be placed inside or beneath the integrated inductors [6]. To enable evaluation of circuits early on in the fabrication cycle, layouts can be developed that require only one layer of metal interconnect.

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