A High Performance 2-GHz Direct-Conversion Front End with Single-Ended RF input in 0.13 um CMOS

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***Abstract* — This paper describes a 2.1-GHz CMOS front-end with a single-ended low noise amplifier (LNA) and a double balanced, current-driven passive mixer. The LNA features an on-chip transformer load to perform single-ended to differential conversion. Implemented in a 0.13 um CMOS process, it achieves 30 dB conversion gain, a low noise figure of 3.1 dB, a 40 kHz 1/f noise corner, an in-band IIP3 of -12 dBm and IIP2 better than 39 dBm, while consuming only 12 mW from a 1.5V power supply.**

I. Introduction

Direct conversion receivers are widely used in wireless receivers for their high level of integration in particular for multi-band front-ends. Critical design issues for a CMOS realization include 1/f noise, DC-offset, and linearity including IIP2. These issues are particularly challenging in transceivers for wireless standards using full duplex communications like WCDMA. Due to transmitter signal leakage into the receiver front-end, very stringent IIP2 requirements must be met. Current solutions use external SAW filters between LNA and mixer to mitigate the effects of the transmitter leakage.

Several highly integrated direct-conversion CMOS front ends [1][2] obtain high IIP2 performance, but at the cost of requiring a fully differential LNA that needs two RF input pins and an external RF single-ended to differential conversion. This typically requires special front-end filters or an additional off-chip balun, which incurs extra loss and degrades the overall noise figure. In practice, power amplifiers, duplexers and antennas are primarily single-ended. Moreover, single-ended RF interfaces reduce the pin count especially in multi-band transceivers.

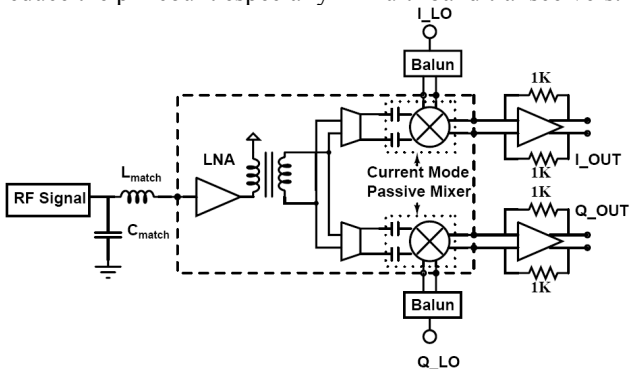

Fig. 1. Block diagram of the front-end.

In this work, we explore the design of high performance 2-GHz CMOS front ends using a single-ended LNA structure (see Fig. 1). The LNA is loaded with an on-chip transformer for single-ended to differential conversion and drives a fully differential RF transconductor. The transcoductor drives a double-balanced, current-mode passive mixer. Passive mixing pairs driven by current input signals and loaded with low impedance created by a transimpedance stage[2] exhibit extremely low 1/f noise and high linearity. This front-end architecture further allows the extensive use of AC coupling which improves the IIP2 performance.

II. LNA with Transformer Load

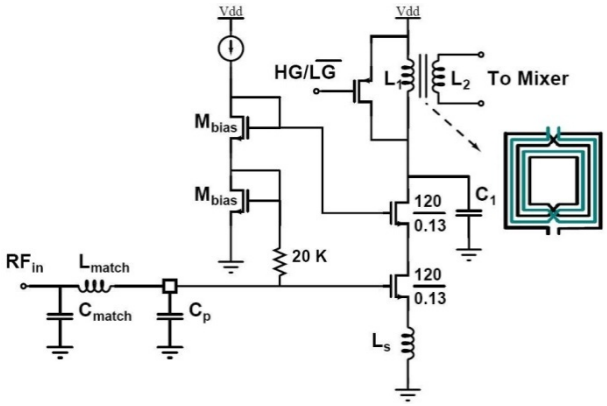

Fig. 2. LNA with on-chip transformer load.

The LNA with an on-chip transformer load is shown in Fig. 2. The single-ended, inductive-degenerated common source amplifier uses a large-size PMOS transistor connected across its output which is turned ON to obtain a low gain mode while maintaining a good input match. In deep submicron LNAs, the noise figure is more strongly affected by losses of the input matching network than by the noise of the active device. Therefore, a high Q off-chip series gate inductor (L_{match}) was used. The parasitic input capacitor, C_p, which is due to the parasitics of the bond pad, bond wire, ESD diodes, and package/board, results in a parallel-to-series downconversion of the real part of the input impedance. An additional external matching capacitor,C_{match}, performs a series-to-parallel impedance transformation and results in a reliable 50 ohm input impedance over temperature and process variations.

To obtain a high front-end IIP2, a double balanced mixer needs to be used, so a single-ended to differential conversion is critical between the LNA and mixer. Additionally, AC coupling is desirable to reject as much as possible the LNA IM2 products which are at low frequencies. An active single-ended to differential conversion is power hungry, and typically suffers from poor common-mode rejection and introduces additional IM2 products. An on-chip transformer load for the LNA gives well-balanced signals, effectively filters out part of the IM2 components generated by the LNA, and consumes no extra power. To achieve a high quality factor, Q, and a high magnetic coupling coefficient, a symmetric, 250um*250um transformer structure was used as shown in Fig. 2. A drawback of using a transformer load is the lower Q and effective impedance of the LNA load compared to what can be achieved with a single inductor in the same area. The lower load impedance requires somewhat larger LNA bias current to maintain gain and noise performance.

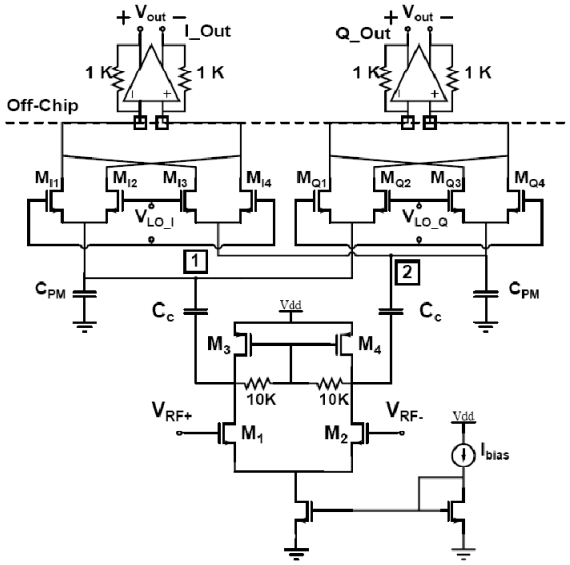

Fig. 3. Balanced transconductor driving the current-mode double-balanced passive CMOS mixer.

III. Current-Driven Passive Mixer

1/f noise and second-order nonlinearity are primary challenges when designing direct conversion receivers. The 1/f noise appears at the output in proportion to the DC bias current through the switched pairs. Therefore passive mixers have much better 1/f noise performance compared to active ones due to the absence of DC bias currents through the mixing pairs. Voltage-driven passive mixers have a substantial voltage swing across the switches, which degrade the linearity performance. A current-driven passive mixer (see Fig. 3) loaded with a transimpedance amplifier load, has negligible signal swings across the switches, which results in significantly better linearity. It is the preferred CMOS architecture for a highly linear, low noise and low power direct-conversion mixer

A balanced transconductor ($M_1 - M_4$) is inserted between the LNA and the I & Q switching quad to increase the effective gain before the switching transistors to improve the front-end noise performance. The conversion gain of the mixer, assuming ideal square wave switching, is similar as for the traditional active switching mixer: $(V_{out+} - V_{out-})/(V_{RF+} - V_{RF-}) = 2/\pi * g_m * R_L$, where g_m is the transconductance of $M_1 and\ M_2$, and R_L is 1 kΩ in this design.

A. Noise Design Considerations

Care has to be taken in the optimization of the switch sizes and bias voltages [4] to avoid an increase of the noise contribution of the baseband amplifier. As shown in Fig. 4, the parasitic capacitance (C_{PM}) at the mixer inputs (nodes 1 and 2), becomes an equivalent switched-capacitor resistor which increases the noise gain for the baseband amplifier's equivalent input noise source $\overline{V_{in,eq}^2}$. The total output noise contribution from the baseband amplifier then becomes:

$$\overline{\mathrm{V_{n,out}^2}} = (1 + 4 * \mathrm{R_L} * \mathrm{f_{LO}} * \mathrm{C_{PM}})^2 * \overline{\mathrm{V_{in,eq}^2}}. \qquad (1)$$

where f_{LO} is the LO frequency. Consequently, the switch size and the AC coupling capacitance (Cc) have to be kept small. Simulations showed that the penalty to the overall front-end noise figure due to this effect is about 0.4 dB.

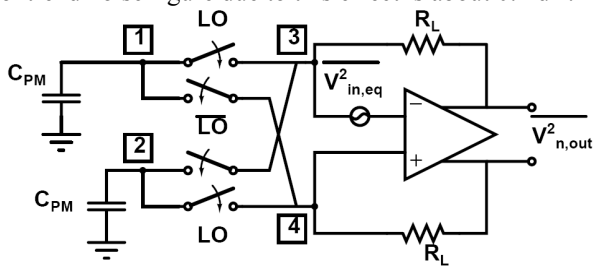

Fig. 4. Transfer of the noise from baseband amplifier to the output through the switched-capacitor input resistance.

A passive mixer can work with either an ON or an OFF overlap region depending on the relative value of the bias voltage at the gate (V_g) to the bias at the source (V_b at node 3 and 4) [3]. During an ON overlap period when all the switches ($M_{I1} - M_{I4}$ & $M_{Q1} - M_{Q4}$) are ON, there is a significant gain of the transimpedance amplifier equivalent input noise voltage, $\overline{V_{in,eq}^2}$ to the output:

$$\overline{\mathrm{V_{n,out}^2}} = \left(1 + \frac{2R_L}{R_{sw}}\right)^2 * \mathrm{V_{in,eq}^2}. \qquad (2)$$

where R_{sw} is the ON-resistance of the switches. Therefore, biasing the switches at OFF overlap mode is desirable

from a noise perspective since it avoids this additional noise transfer.

B. Second-order Nonlinearity Design Considerations

The single-ended LNA generates low-frequency IM2 components which are (partially) converted to differential but also significantly attenuated by its output transformer. The LNA IM2 components are further attenuated by the AC coupling capacitors (Cc) before the mixer switching pairs (Fig. 3). The mixer transconductor generates large common-mode (CM) IM2 components, but its differential-mode (DM) IM2 components are only set by device mismatches and thus relatively small. Also these IM2 components are attenuated by the AC coupling capacitors (Cc) before reaching the switching transistors.

The current-mode passive mixer has a fully differential topology so that its contribution to the output IM2 products again depends only on mismatches in the devices. Moreover the circuit topology assures a small voltage swing across the switching devices so that their non-linearities are intrinsically small.

Ideally, there is no low-frequency feed through for differential input currents in a balanced current-mode passive mixer and there is no CM-to-DM conversion. However, in practice, due to mismatches in the switching pair transistors, a feed through of the low frequency DM IM2 components from the LNA and mixer transconductor appears, and, additionally, a partial conversion of CM IM2 components to DM IM2 components takes place. These CM IM2 components are very large compared to the other IM2 contributions, so this CM-to-DM conversion due to mismatches in the switching pairs is a primary design consideration. A similar CM-to-DM conversion occurs due to mismatches in the transimpedance amplifier load resistors, but resistors with sufficient matching can be laid out on chip. In this work, we used an off-chip transimpedance amplifier with high quality matched SMD load resistors.

Using a similar analysis technique as in [5], we can model the device mismatch in a switch pair by means of an equivalent offset voltage connecting to the gate of one of the switches. For both ON and OFF overlap, the actual gating function, p', through the switch with offset can be decomposed into the ideal gating function, p, for zero mismatch plus a train of impulses, p_m, due to the presence of mismatch. Fig. 5, for example, shows the case of OFF overlap. The extra impulses p_m in the gating function of the switch with mismatch are not present in the gating function of the other switch and thus result in an imbalance. Note that p_m has a non-zero DC component. Consequently, a DM-to-DM low-frequency feed through occurs as well as a low-frequency CM-to-DM conversion. The resulting low-frequency leakage, L, is then:

$$\mathrm{L} = \frac{2*\mathrm{V_{offset}}}{\mathrm{T_{LO}}*\mathrm{S_{LO}}}. \quad (3)$$

where V_{offset} is the offset voltage, T_{LO} is the period of the LO signal, S_{LO} is the slope of the LO voltage at the switching time. Although it is desirable to use switch transistors with a large area to improve their matching, the devices cannot be made too large to avoid an excessive transimpedance amplifier noise penalty, as described earlier. Note that for a sinusoidal LO drive, S_{LO} reaches maximum when V_g is close to $V_b + V_{th}$ and, additionally, increasing the LO amplitude will increase S_{LO}. We conclude that for a passive mixer, the choice of the gate DC bias voltage plays a role in determining its low frequency DM signal feed through and its CM to DM conversion and thus the overall front-end IIP2 performance. Taking noise effects into account, it is preferable to bias the switches with small amount of OFF overlap.

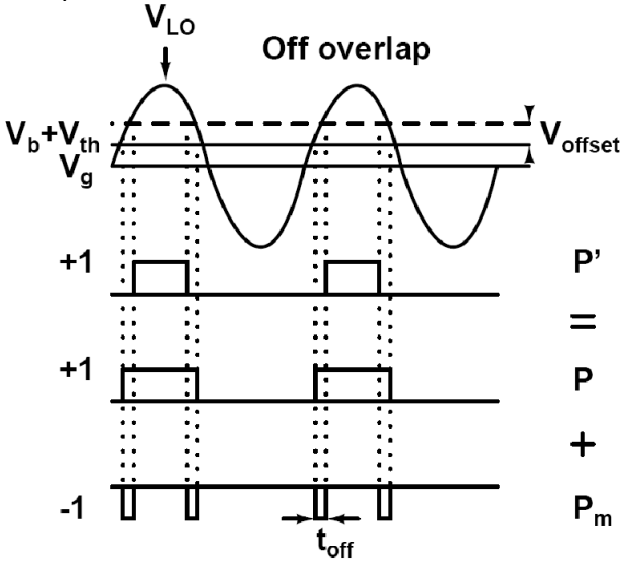

Fig. 5. The effect of switch bias on IIP2 for passive mixer.

IV. IC Implementation And Measurement

The photograph of the IC prototype is shown in Fig. 6. Great care has been taken to symmetrically lay out both active and passive devices. The transformer is using a patterned ground shield to reduce the electric field substrate losses and the top two metal layers were strapped to reduce the inductor' parasitic resistance. The IC was implemented in a 0.13-um CMOS process and occupies a chip area of 1.1 mm^2. The chip was packaged in a QFN24 package and tested on a FR4 board.

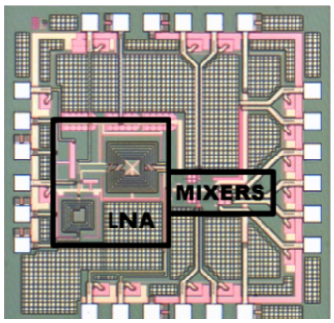

Fig. 6. Die photo of the front-end prototype.

The whole circuit consumes 8mA from a 1.5 V supply. With the LO frequency at 2.14GHz, we have measured the S_{11}, conversion gain, noise figure, IIP2 and IIP3 of the LNA/Mixer chain. Table 1 summarizes the measured performance.

Fig. 7 shows the noise figure versus output frequency in the high gain and low gain modes measured using the Noise-Figure personality of the Agilent E4446A spectrum analyzer, together with the simulation results. In the frequency range from 100 kHz to 2 MHz, the power spectral density of the output noise in the high gain mode is white and is about 0.5 dB higher than simulation value (2.6 dB). This discrepancy is largely caused by a lower gain in the actual circuit due to a modeling inaccuracy of the transformer loss. The transformer loss was verified with a dedicated probing test structure.

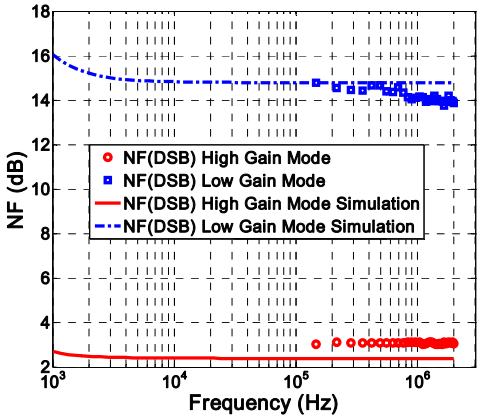

Fig. 7. NF(DSB) for High Gain Mode and Low Gain Mode.

The 1/f noise corner could not be determined using the noise figure personality of the spectrum analyzer due to a lower frequency limit of 100 kHz. Instead the 1/f noise corner was observed directly from the spectrum analyzer output by terminating the LNA input with 50Ω and was measured to be at 40 kHz.

Four test chips were mounted on boards and their IIP2 performance was determined to be 39, 42, 42 and 47dBm respectively without any LO phase and amplitude calibration. A gate switch bias lower than the source voltage plus the threshold voltage to operate with OFF overlap indeed offered the best IIP2 and noise performance.

TABLE 1. RESULTS AND PERFORMANCE COMPARISON.

	This Design				[6]	[7]	[1]	[2]
	High Gain		Low Gain		High	High	High	High
	Mea.	Sim.	Mea.	Sim.	Gain	Gain	Gain	Gain
Single Ended Input	Yes				Yes	Yes	NO	NO
Conversion gain [dB]	30	33	15	14	33	28.4	31.5	29
DSB Noise Figure [dB]	3.1	2.6	15.7	15.9	4.3	3.2	3.5*	4.4*
1/f corner [kHz]	40	10	40	10			15	70
IIP3 [dBm]	-12	-15	-3	-3	-14.5	-17.5	-10.5	-1
IIP2 [dBm]	>39		>47		34	15	>51	35(avg.)
S11 [dB]	-22	-23	-27	-24	<-18	-17.8		
Supply [V]	1.5				1.8	2.7	0.75	1.8
Power [mW]	12				22.5	27**	11.25	15
Die Area [mm*mm]	1.1				3.5		2.7	4.4
Technology	0.13um				BiCMOS	BiCMOS	0.09um	0.18um
Frequency	2G				2G	2G	2G	2G

*Needs off-chip single-ended to differential conversion.
**Excluding the power from LO buffers for fair comparison.

V. DISCUSSION & CONCLUSIONS

The performance of the presented single-ended input CMOS direct-conversion front-end compares favorably with other state-of-the-art, single-ended input BiCMOS and differential-input CMOS designs, which demonstrates the effectiveness of the presented front-end circuit architecture and design methodology. The single-ended input simplifies the PCB design and avoids additional noise figure degradation from an external single-ended to differential conversion.

ACKNOWLEDGMENTS

The authors would like to thank Toshiba Corporation for financial support and chip fabrication; S.Kapur and D.Long of Integrand Software for the use of the EMX simulation.

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