20.6 A 0.6V 32.5mW Highly Integrated Receiver for 2.4GHz ISM-Band Applications

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We explore the challenges of designing RF transceivers for an ultra-low-voltage (ULV) supply with performance that is compatible to commercial standards. The ITRS roadmap projects that the aggressive device size scaling will result in supply voltage reductions to well below 1V, in particular for low-power technologies. The use of alternative energy sources also requires ULV operation in some applications. Achieving sufficient linearity with low power consumption is very challenging for the ULV mixer and baseband circuits. The on-chip LO generation and distribution is difficult due to the low-voltage device bias. We present optimized mixer and filter topologies, and a polyphase LO buffer, used in a low-power ULV receiver for 2.4GHz applications like Bluetooth or Zigbee. The use of spiral inductors is kept to a minimum to avoid their excessive area. The design techniques demonstrated here can enable the continued integration of RF front-ends onto SoC devices in nano CMOS technologies without requiring dedicated supply voltages or thick oxide devices.

The block diagram of the receiver prototype is shown in Fig. 20.6.1. All RF and analog baseband components and the LO synthesizer are on-chip. The single-ended inductively degenerated common-source LNA has two gain mode settings (Fig. 20.6.2); its output is AC-coupled to one input of the double-balanced switched-transconductor I/Q mixers [1] while the other input is biased at AC ground. The differential downconverted signal current is fed into the virtual ground of the first biquad in the baseband section, which is configured as a transimpedance amplifier with filtering. The first voltage conversion of the downconverted signal thus happens after a filtering step which reduces the out-of-channel blockers by at least 10dB.

In low-IF receive mode, used for standards with narrow signal band, such as Bluetooth, the 6th-order channel-select filter (Fig. 20.6.1) is configured as a complex band-pass filter centered at 1MHz. For standards with wider signal-bands, such as Zigbee, the baseband filter is configured as a low-pass filter to support a zero-IF receive mode. An active-RC biquad filter is implemented (Fig. 20.6.3) because of its higher loop-gain compared to leap-frog type filters, thanks to the second integrator in the loop. The biquad implementation also allows easy distribution of gain and filtering to optimize noise and linearity performance. The biquad (Q=0.5) offers an attenuation of 10dB in the stopband and hence is placed first to reject the out-of-band blockers. The biquad (Q=2) has less out-of-band rejection, but improves the filter flatness in the passband and is therefore used at the end. To avoid high sensitivity of the transfer function to passive element values, a 6th-order Butterworth filter is used with a maximum pole Q of only 2. To convert a low-pass biquad into a complex band-pass, the I and Q paths are coupled using resistors (Fig. 20.6.3). The filter poles are realized using high-resistivity poly resistors and MOM capacitors that are scaled in each biquad depending on noise requirements. The filter is tuned digitally by switching capacitors. The variable gain stage is integrated with the second biquad and is controlled digitally by switching input resistance of the biquad (Fig. 20.6.3). The baseband gain can be varied from 0 to 24dB in steps of 6dB.

The quadrature LO signal is generated on-chip using a fractional-N frequency synthesizer operating at twice the LO frequency (Fig. 20.6.1). A tail biased 4.8GHz VCO with an output common mode of 0.6V uses a 1.5nH on-chip M8/M9 center-tapped inductor with a Q of 12. Switched MOM capacitors and switched inversion-mode MOS varactors center the VCO at the desired channel. With the analog tuning varactor a span of 80MHz can be covered with a tune voltage between 50mV and 550mV from the charge pump. A first fixed 4.8GHz divide-by-2 creates clocks to trigger the programmable divider and the retiming flip-flop. The divide-by-2 uses pseudo-differential SCL latches for additional headroom. It is biased for a weak self-oscillation at 2.4GHz and is injection locked by the large VCO signal. The programmable divider uses cascaded SCL and CMOS divide-by-2/3 cells and modulus extension logic [2]. A 24b MASH-1-1-1 $\Delta\Sigma$ modulator controls the divider modulus; steps as small as 2Hz can be achieved from a 32MHz reference over a synthesizable range from 2.2 to 2.6GHz.

The differential I/Q LO signals are provided by a second fixed 4.8GHz divide-by-2 which uses resistive averaging to further equalize the phases feeding the polyphase LO buffers. To avoid coupling between the RF front-end and the LO synthesizer, they are separated in the layout. The LO has thus to be distributed over fairly long distances, and needs to be buffered multiple times to maintain a large swing (Fig. 20.6.2). After the signal is sufficiently amplified with two common-source amplifiers, it is passed through a single-stage active polyphase filter [3] to correct any quadrature error that might have occurred due to mismatches. The final buffer stage drives the common sources of the transconductors in the mixer with a rail-to-rail LO signal.

The highly integrated receiver is designed with regular V_T devices in a standard 90nm CMOS process (see Fig. 20.6.7 for a die micrograph). The single-ended RF input is applied to the LNA and the output is taken from the differential I_{OUT} and Q_{OUT} (Fig. 20.6.1) outputs. Figure 20.6.4 shows the measured receiver conversion gain (67±0.8dB), S_{11} (<–18dB) and noise figure (16±0.25dB) over the 2.4 to 2.48GHz input band. An IIP3 of –10.5dBm is obtained for out-of-channel tones at 1MHz and 2MHz offsets. The output 1dB compression point is +3dBm. It should be noted that in its current implementation the receiver has a programmable gain range of 33dB. This range can be extended with additional gain switches in the baseband biquads without any power penalties. This will improve the handling of large in-band signals beyond the current –30dBm. Figure 20.6.5 shows the complex band-pass filter frequency response for different gain settings and the tuning characteristics; an image rejection of at least 32dB is achieved for a 1MHz IF. The filter bandwidth is discretely tunable from 400kHz to 2.5MHz in the band-pass mode and from 900kHz to 2MHz in the low-pass mode in steps of 30kHz (not shown). The total amplitude and phase mismatch between I_{OUT} and Q_{OUT} is measured to be smaller than 0.06dB and 2° in low-pass mode with a sinusoidal RF input. The LO phase noise at 3MHz offset is –127dBc/Hz, the spur level is –50dBc at 32MHz offset and the integrated rms phase error is less than 2.9°. The receiver performance over a voltage supply range from 0.55 to 0.65V and for different gain settings is summarized in Fig. 20.6.6. The achieved performance is compatible with ISM-band applications such as Bluetooth and Zigbee.

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[1] E. A. M. Klumperink, S. M. Louwsma, G. J. M. Wienk and B. Nauta, "A CMOS Switched Transconductor Mixer," *IEEE J. Solid-State Circuits*, vol. 39, no. 8, pp. 1231-1240, Aug. 2004.
[2] S-A. Yu and P. Kinget, "A 0.65V 2.5GHz Fractional-N Frequency Synthesizer in 90nm CMOS," *ISSCC Dig. Tech. Papers,* pp. 304-305, Feb. 2007.
[3] F. Tillman and H. Sjöland, "A Polyphase Filter Based on CMOS Inverters," *NORCHIP Conference*, pp. 12-15, Nov. 2005.

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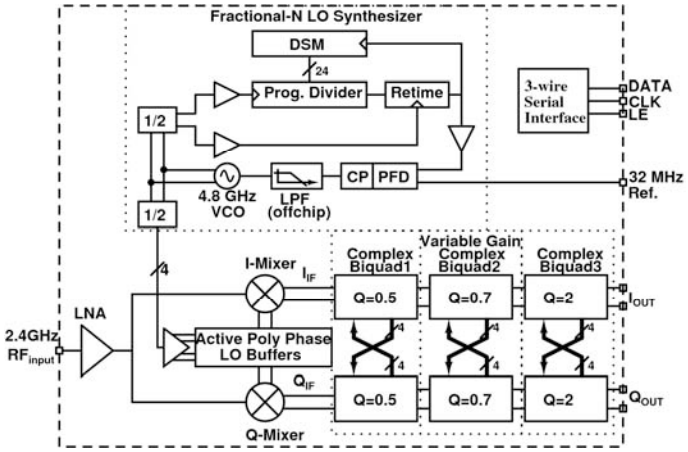

Figure 20.6.1: Block diagram of the receiver.

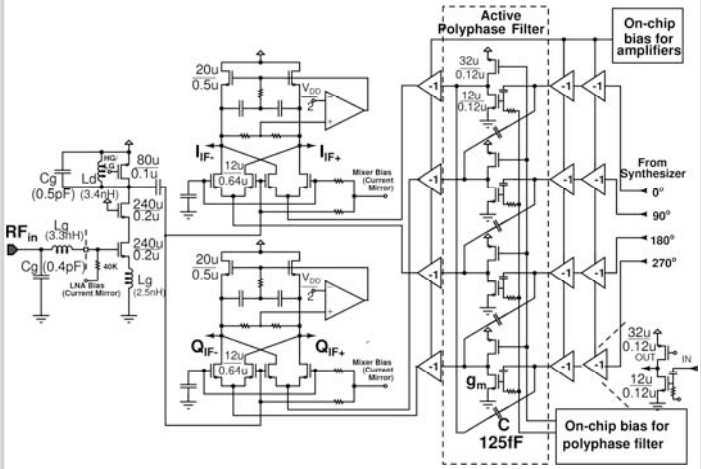

Figure 20.6.2: LNA, mixer and active polyphase LO buffer schematics.

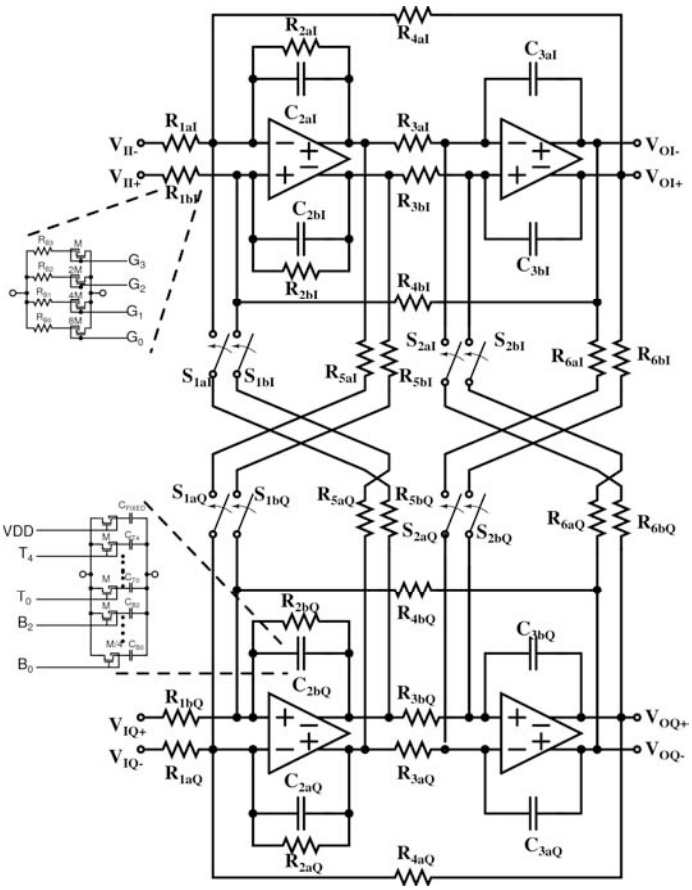

Figure 20.6.3: Schematic of the complex biquad section. The first biquad is a transimpedance stage and does not have the input resistors R_{1aI}, R_{1bI}, R_{1aQ}, and R_{1bQ}.

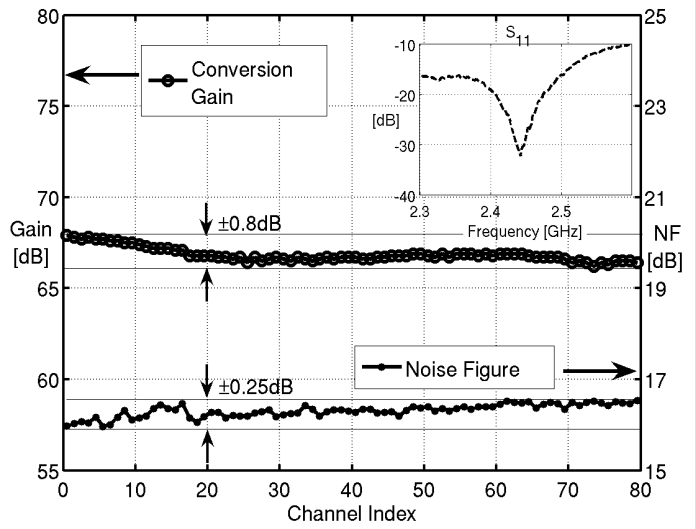

Figure 20.6.4: Measured receiver conversion gain and noise figure for 80 1MHz channels from 2.4 to 2.48GHz.

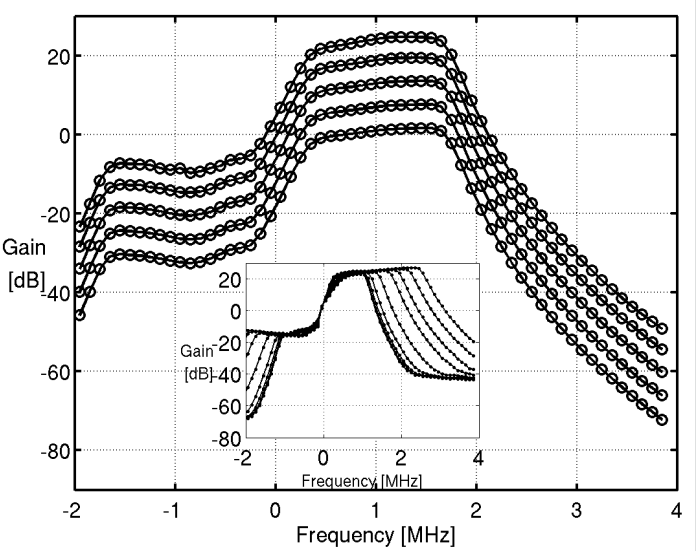

Figure 20.6.5: Frequency response for the low-IF receiver mode with a 1MHz IF.

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Supply	[V]	0.55	0.60				0.65
Gain Setting Front end gain Baseband gain		Max. Max.	**Max.** **Max.**	Max. Min.	Min. Max.	Min. Min.	Max. Max.
	[dB]	66	**67**	44	56	33	67
Noise Figure	[dB]	18	**16**	17	27	28	16.5
IIP3	[dBm]	-12	**-10.5**	-8.5	-2.5	-2	-10
Image Rejection	[dB]	32	**32**	32	35	35	32
LO Synthesizer Phase Noise at 3MHz offset	[dBc/Hz]	-125.9	**-127.1**				-127.5
Power Dissipation: LNA Mixers LO Buffers Synthesizer Baseband Filters	[mW]	29 2.7 0.9 9 11 5.4	**32.5** **3** **1** **10** **12.5** **6**				36 3.3 1.1 11 14 6.6
Package		**64pin QFN**					
Technology		**90nm CMOS (RVT devices)**					
Area (including pads)	[mm²]	**2.9**					

Figure 20.6.6: Receiver performance summary.

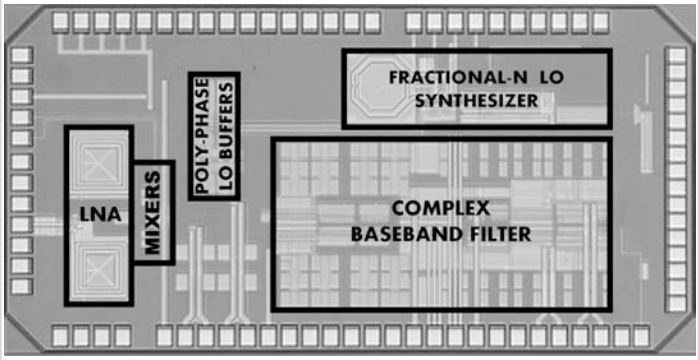

Figure 20.6.7: Die micrograph.

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