Synthesis of Optimal On-Chip Baluns

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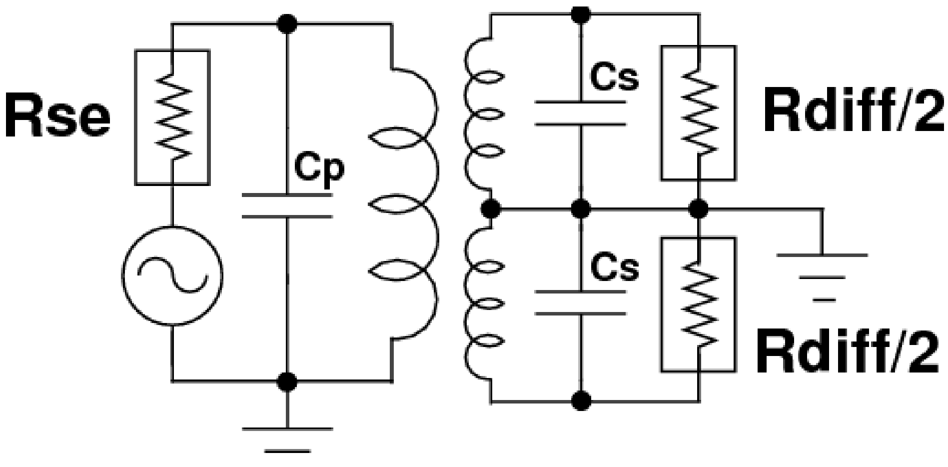
Outline

- Introduction
- Motivation for using on-chip baluns
- Synthesis of optimal baluns
  - EM simulation
  - Scalable model generation
  - Model tuning and optimal synthesis
- Measurement and verification
- Conclusions

Balun introduction

- Baluns and transformers are important components found in mobile phones and other wireless devices.
- A **balun** is a passive component that transforms power from a **BAL**anced to an **UN**balanced port.
- In most cases, baluns also perform impedance transformation.
- Composed of a transformer and tuning capacitors

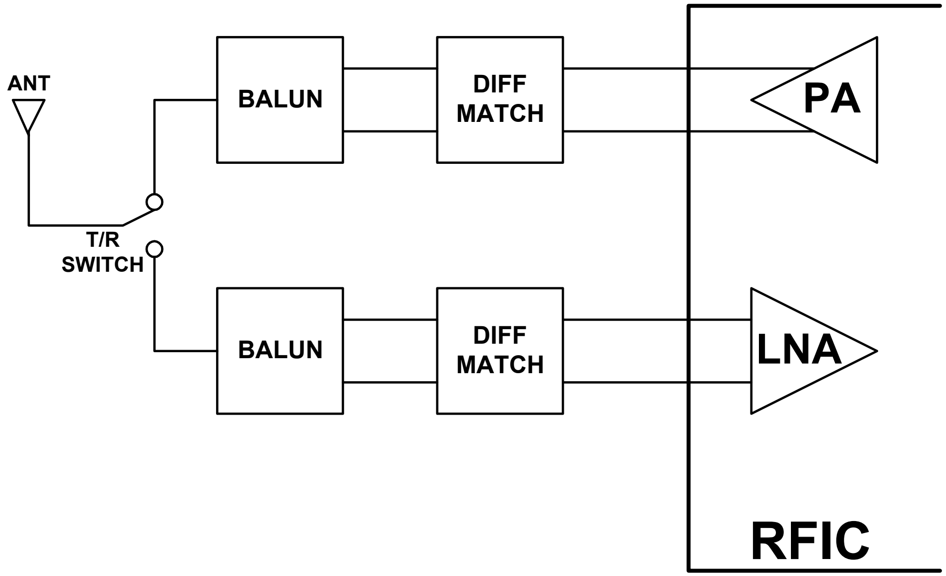


Rse=50 Ohms
Rdiff=200 Ohms

Baluns introduction...

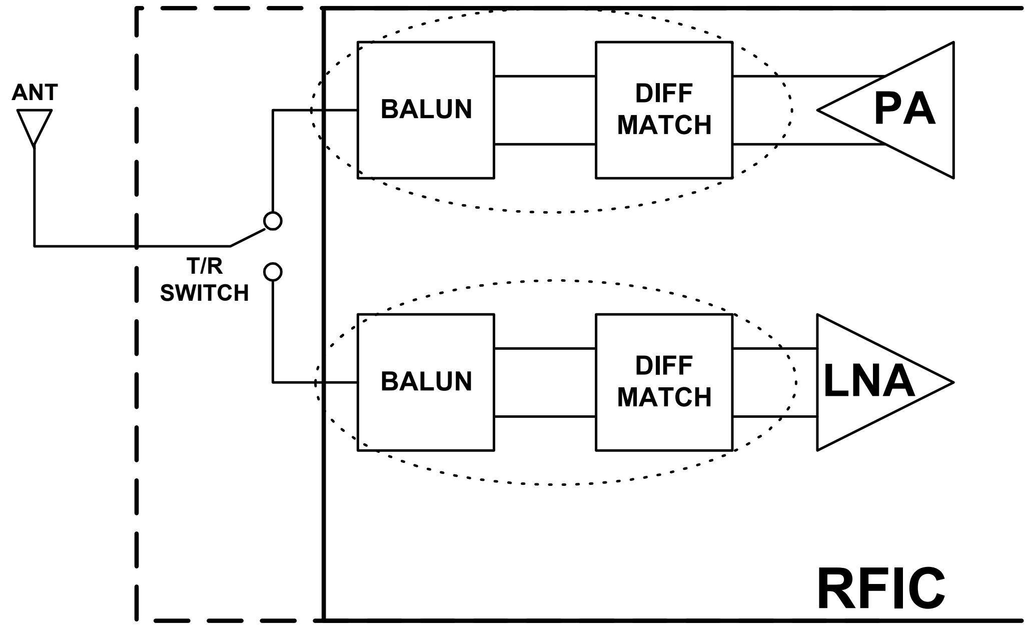
- Key figures of merit:
  - Differential to single-ended insertion loss.
  - Differential (balanced) input impedance (return loss).
  - Single-ended (unbalanced) input impedance (return loss).
  - Imbalance is often measured as maximum amplitude and phase imbalances.
- Basic baluns (e.g. 50Ω-50Ω, 50Ω-200Ω etc.) used conjugate matched ports with real impedances.
- Advanced baluns may have complex port impedances.

Conventional RF Front-End Configuration



- RFIC circuit architecture is typically differential
- Antennas and board level RF configurations are single-ended
- One or two baluns are required in the front end
- Conventional front-end configuration uses an external balun to convert to single-ended transmission line.
- Matching networks required between the balun and RFIC

Integrated Balun/Match



- Integrated baluns are custom-designed to match both unbalanced and balanced impedance levels.
- They merge the functionality of the balun and matching network into a single circuit.
- They also make it possible to integrate the T/R switch in some cases.

Why on-chip?

- Balun loss directly impacts noise figure and power efficiency
- Traditionally baluns have been off-chip ceramic components
- With thick metal copper, high resistivity substrates and good design techniques we can now fabricate better on-chip baluns than off-chip baluns while requiring significantly less area

	Ceramic Baluns (Murata, TDK)	On-Chip Baluns (UMC)
Insertion Loss	1dB-1.5dB	1dB-1.5dB
Phase Imbalance	10 degrees	< 0.25 degrees
Amplitude Imbalance	0.5dB	< 0.1dB
Area	Large (2mm x 1.2mm)	Small (300μm x 300μm)
Yield	Large process variation and low yield	Low process variation and high yield, better integration

Optimal balun syntheis

I. Create an automated layout generator

II. Run EM simulations over the design space

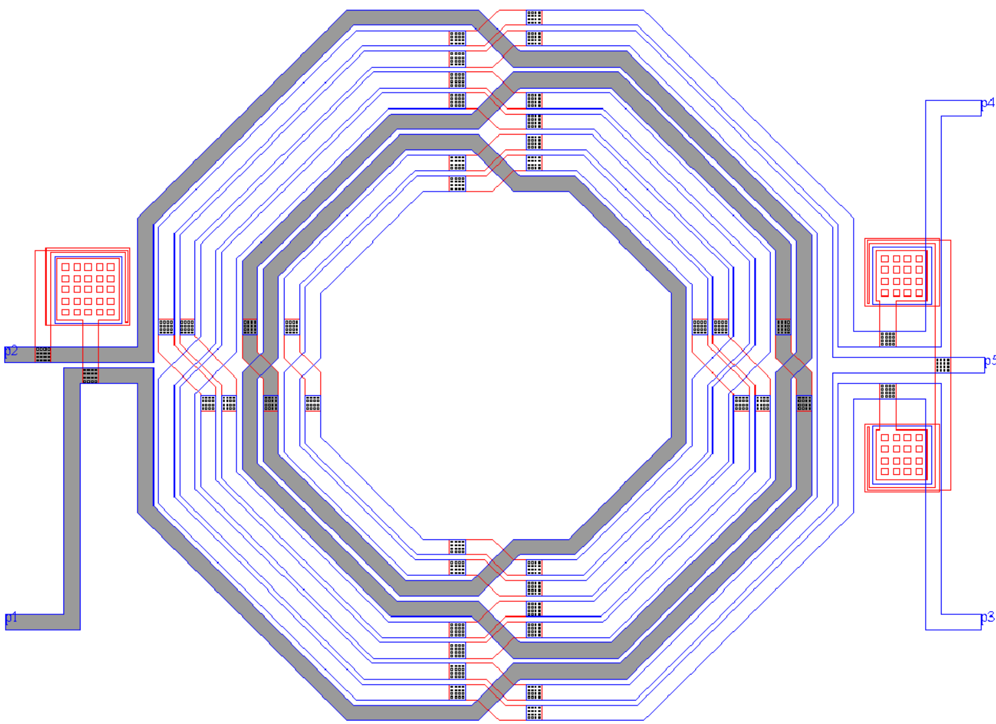
III. Create a scalable model

IV. Use an optimizer to determine the optimal layout and tuning capacitor values

- Steps I, II and III are one time, pre-characterization steps that are technology dependent

Layout generation

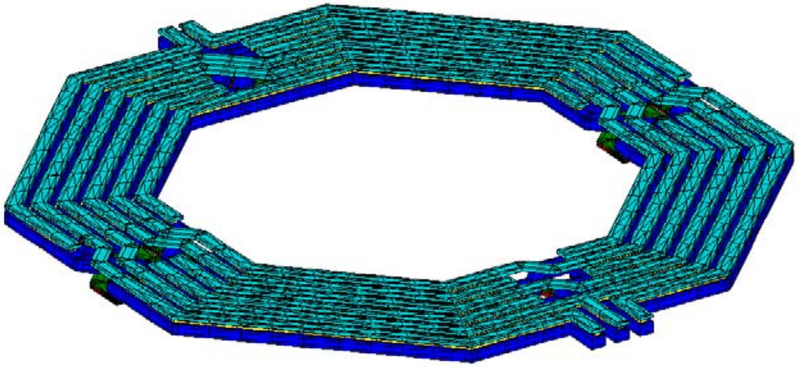
- Parameterized layout generator for transformers
- The design space
  - turns ratio (1:1 – 1:4)
  - number of turns (2-5)
  - width (4μm-10μm)
  - outer diameter (50μm-400μm)
- Create about 1000 transformer layouts
- A sample 1:2 transformer layout. The layout also shows the tuning MIM capacitors used



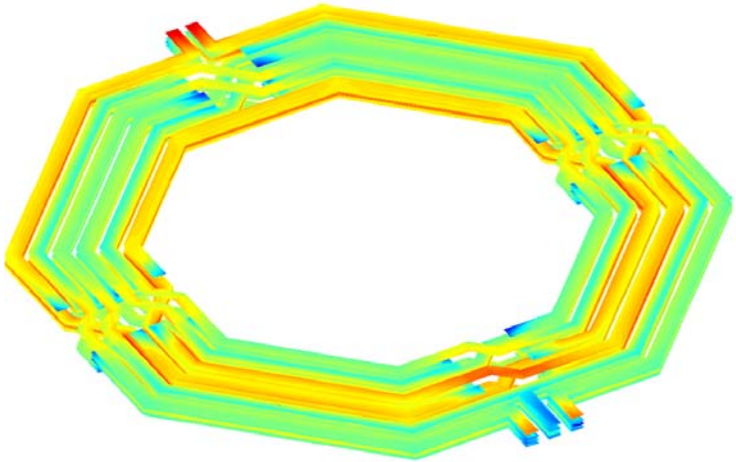
EMX 3D electromagnetic solver

$$E_s(r) = \frac{1}{\sigma} J(r) + j\omega A(r) + \nabla \phi(r).$$

- Physical Effects on ICs
  - R, L, C and Substrate effects unified and fully coupled
- Inductance
  - Distributed 3D volume currents
- Resistance
  - Skin effect and volume loss
- Capacitance
  - Accurate sidewalls of MOM caps
  - Thin-film MIM caps
- Substrate
  - Multi-layered lossy substrate
  - Substrate doping and bias



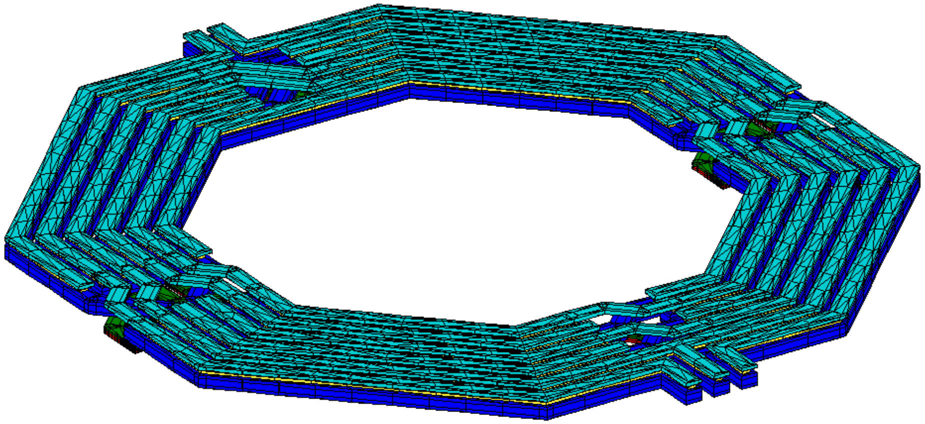
3D Mesh of Balun



current flow

EMX uses an FMM-based fast matrix solver

- Integral Equation-based 3D EM Field Solver
  - Preconditioned iterative methods
  - New "Full-Wave" FMM
  - Layout-regularity exploited
  - Adaptive Fast Frequency Sweep using Krylov subspace techniques
  - See *"Large-scale full-wave simulation", DAC 2004, Kapur and Long.*
- Speed
  - 2 orders of magnitude faster than finite-element tools
  - 1 order faster than BEM
- 1000 Balun simulations run overnight

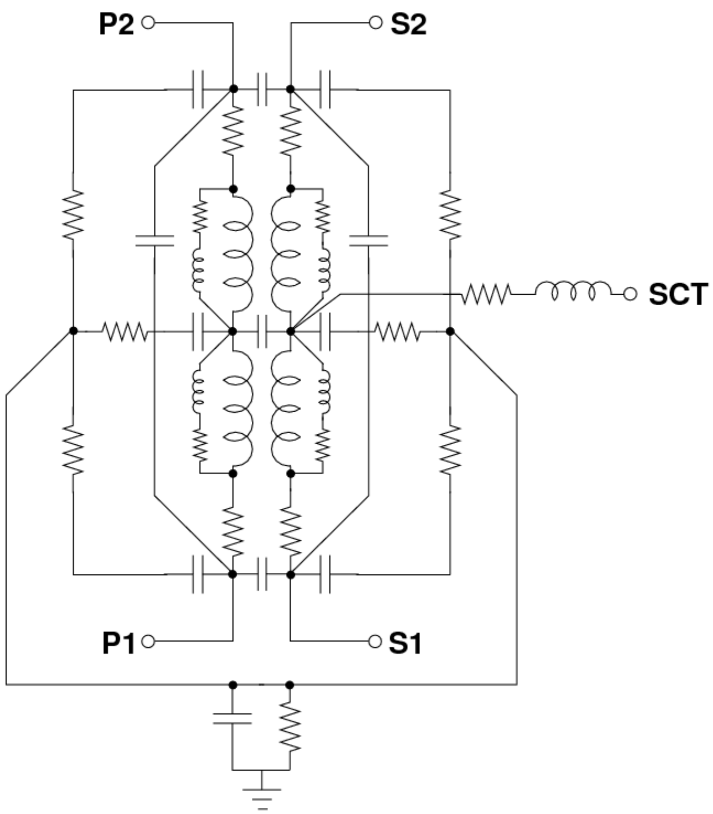


Freq. Range	Freqs	Basis functions	Time	Mem
2.5GHz	1	26,662	90s	160MB
DC-10GHz	200	26,662	307s	330MB

Intel Xeon
2.33 GHz, 16 GB RAM

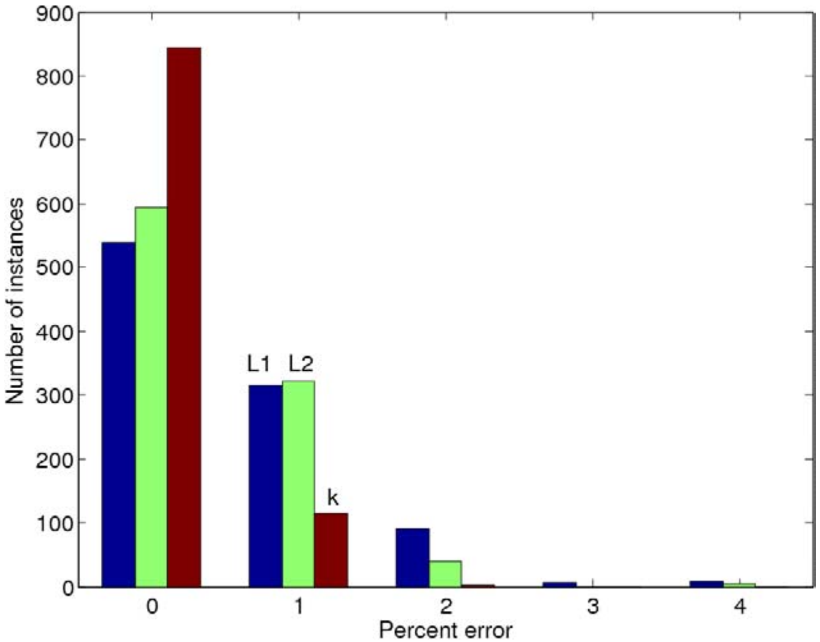
Building a scalable transformer model

- The topology for the scalable model was derived from intuition
  - Two center-tapped coils
  - Each coil has additional resistors and inductors for modeling skin effect
  - Combination of resistors and capacitors model the substrate
  - Each element has a value that is a non-linear function of the geometric parameters
  - The specific form is based on physical intuition (e.g., main series resistance is proportional to diameter and inversely proportional to width)



Using Continuum for Model synthesis

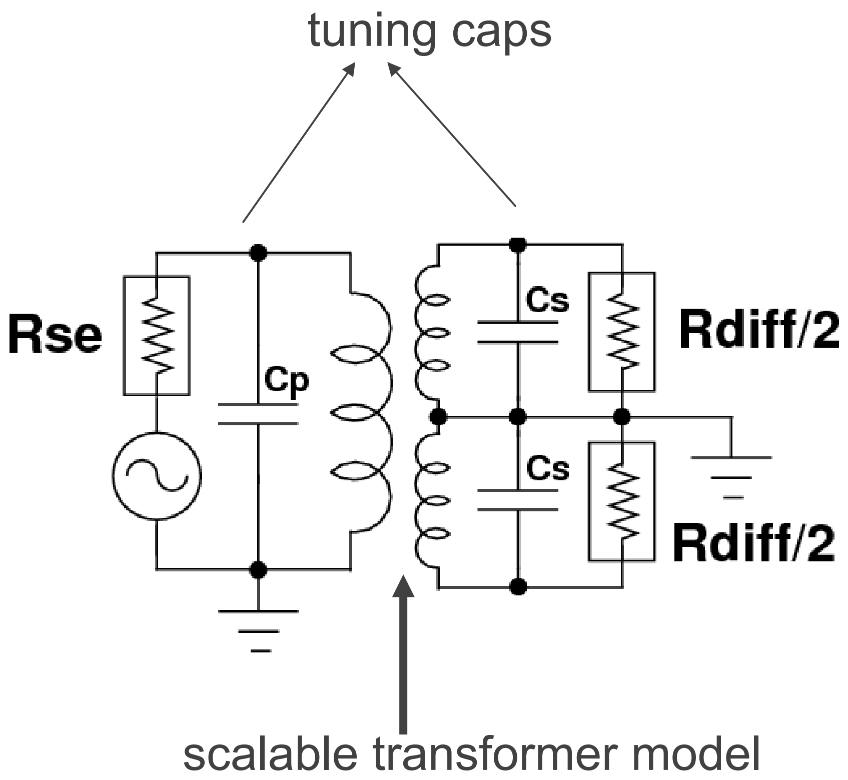
- The program Continuum was used to build the scalable transformer from the 1000 S-parameter files
- Continuum uses
  - a specialized non-linear, least squares optimizer
  - Special circuit based constraints are used to ensure passivity (R, L, C > 0 and the matrix corresponding to k values needs to be positive definite)
  - an objective function that included S-parameters from the simulation as well as derived metrics such as insertion loss
- Error histogram shows < 2% error model vs simulation



Model playback vs simulation

Optimal Balun synthesis

- A separate program called the Optimal Transformer Finder (OTF) was developed
- Given a scalable model of a transformer and load impedance characteristics obtains "optimal" tuning capacitors to insertion loss
- This program takes a few seconds to find the optimal balun (transformer)
- Can be used to trade-off insertion loss vs silicon area
- The baluns are "optimal" for a given layout style and design space

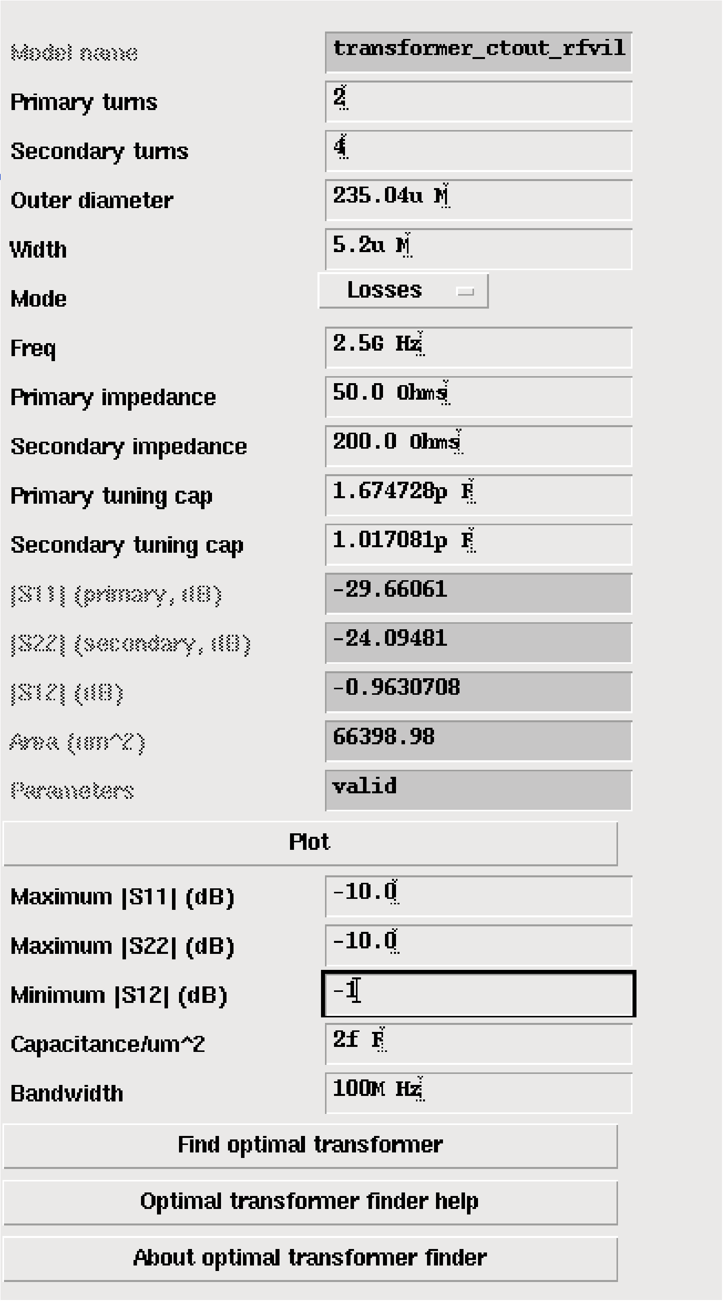


Designing a balun for optimal insertion loss

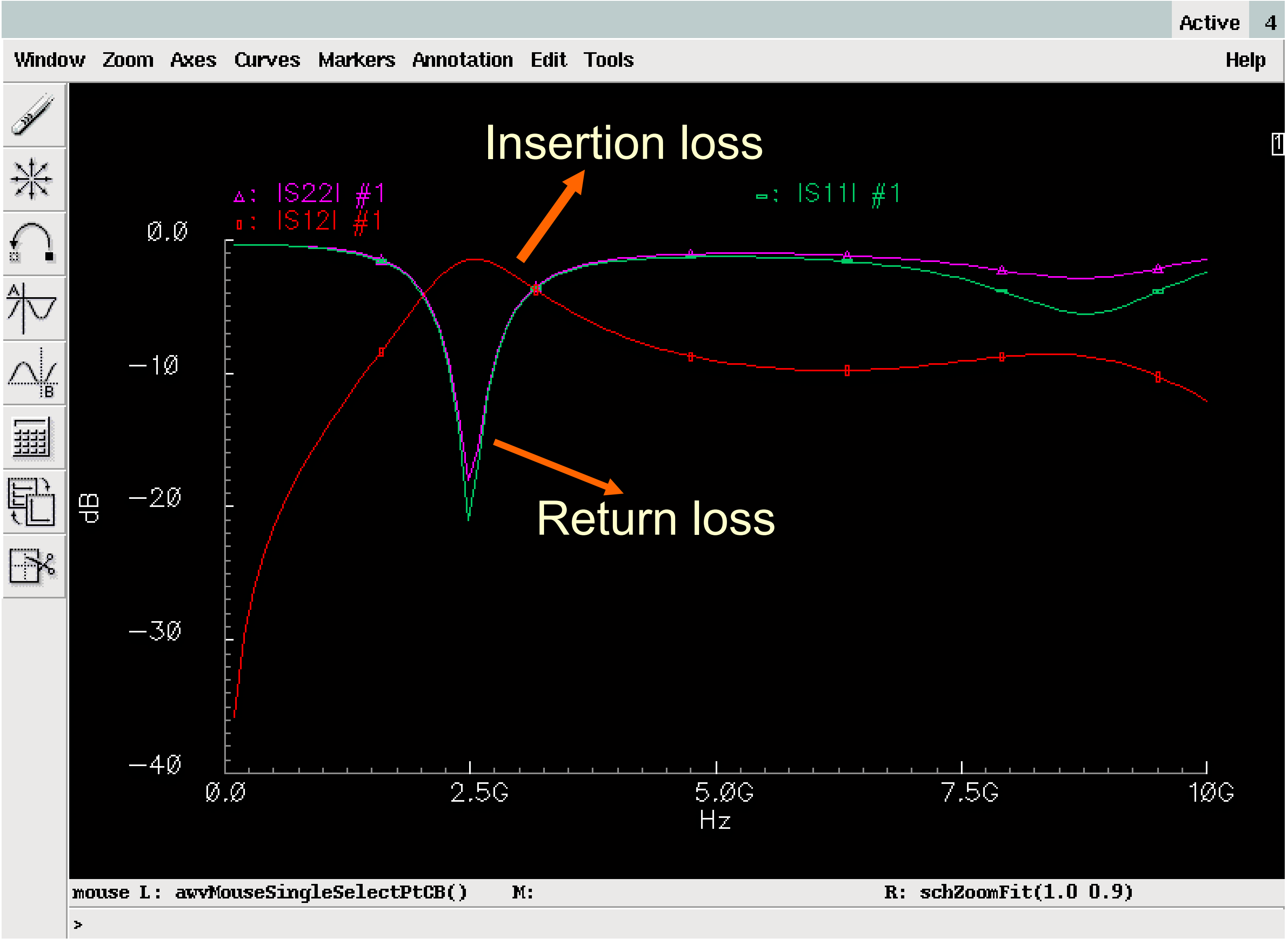
- The designer specifies the input and output impedances,
  - Input impedance of package
  - Output impedance of driver
- The OTF then finds
  - the optimum transformer
  - associated tuning capacitors that satisfy the loss constraints
- The most important design is a balun which has a single-ended input and a differential output
  - Primary is not center-tapped
  - Secondary is center-tapped

Designing an 802.11B balun

- Design a single-ended to differential balun with center-tapped output using the following constraints
  - 50 Ohms input impedance
  - 200 Ohms output impedance
  - Minimum insertion loss of −1dB
  - Maximum return loss of −10dB
- OTF determines
  - Balun geometry
  - Input and Output MiM capacitor values to tune the balun
  - Minimize area (including MiM area)



Plotting insertion and return losses

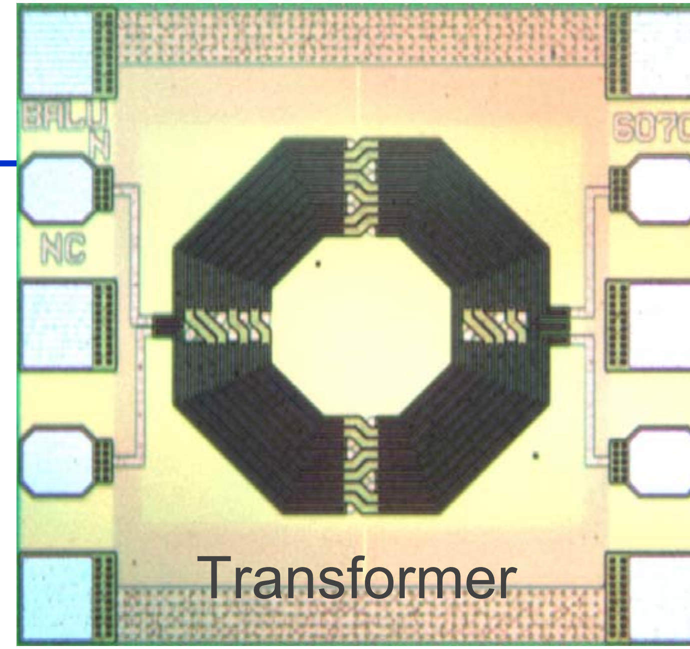


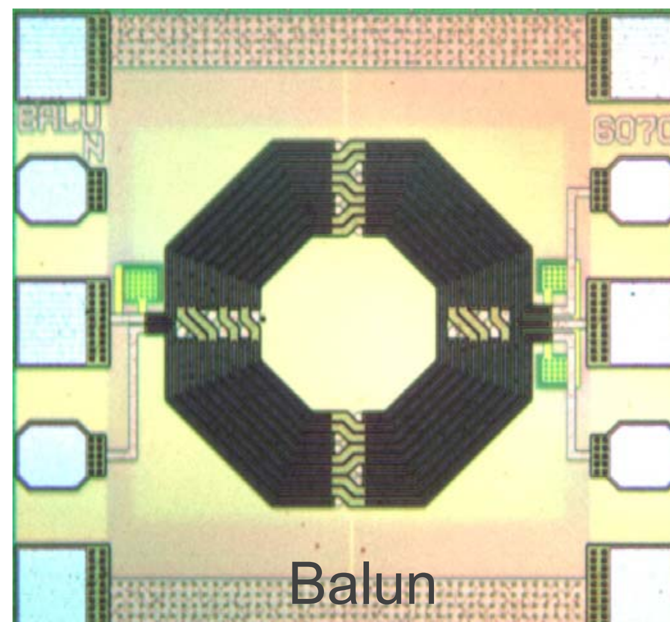
Measurement and verification

- The technique described was used to design 4 commonly used 2:1 baluns with single-ended input impedance 50Ω and differential output impedance of 200Ω
  - 802.11A (5115-5825MHz)
  - 802.11B (2400-2483MHz)
  - DCS (1710-1880MHz)
  - GSM (824-915MHz)
- The devices were fabricated by UMC on a standard 90nm, 9 level Copper metal process with 3μm thick metal for the top metal and substrate resistivity of 20 Ohm-cm
- Tuning MiM capacitors of about 2fF/square micron used

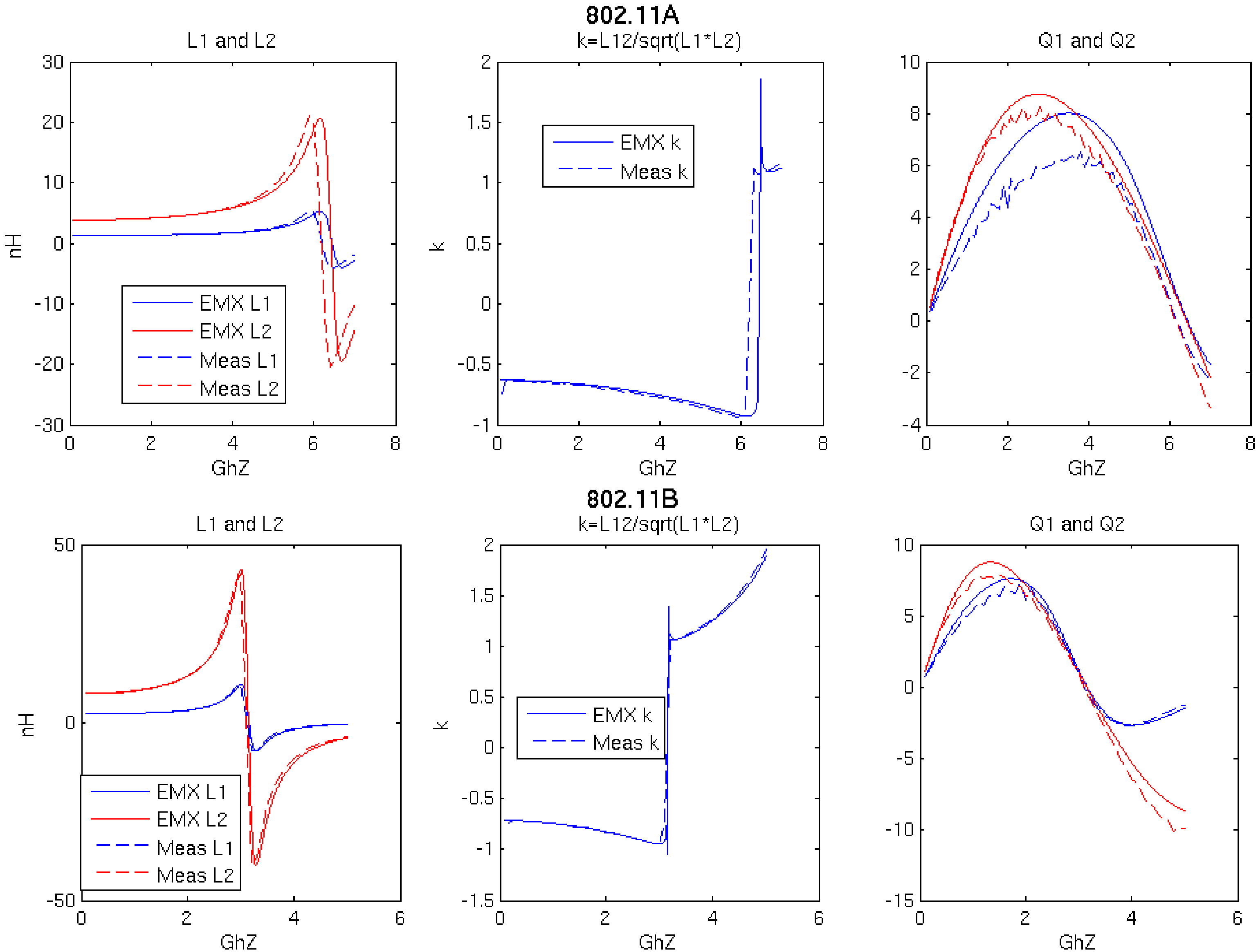
Measurement setup

- For verification two separate sets of layouts
  - 4 transformers
  - 4 baluns
- Four-port measurements were obtained using an Agilent PLTS 50GHz characterization network analyzer.
- For the purposes of verification,
  - all devices were considered to contain the leads up to the edge of the pad frame.
  - This allowed us to use only an open de-embedding and still have minimal de-embedding artifacts.





Transformer plots EMX vs Measurement



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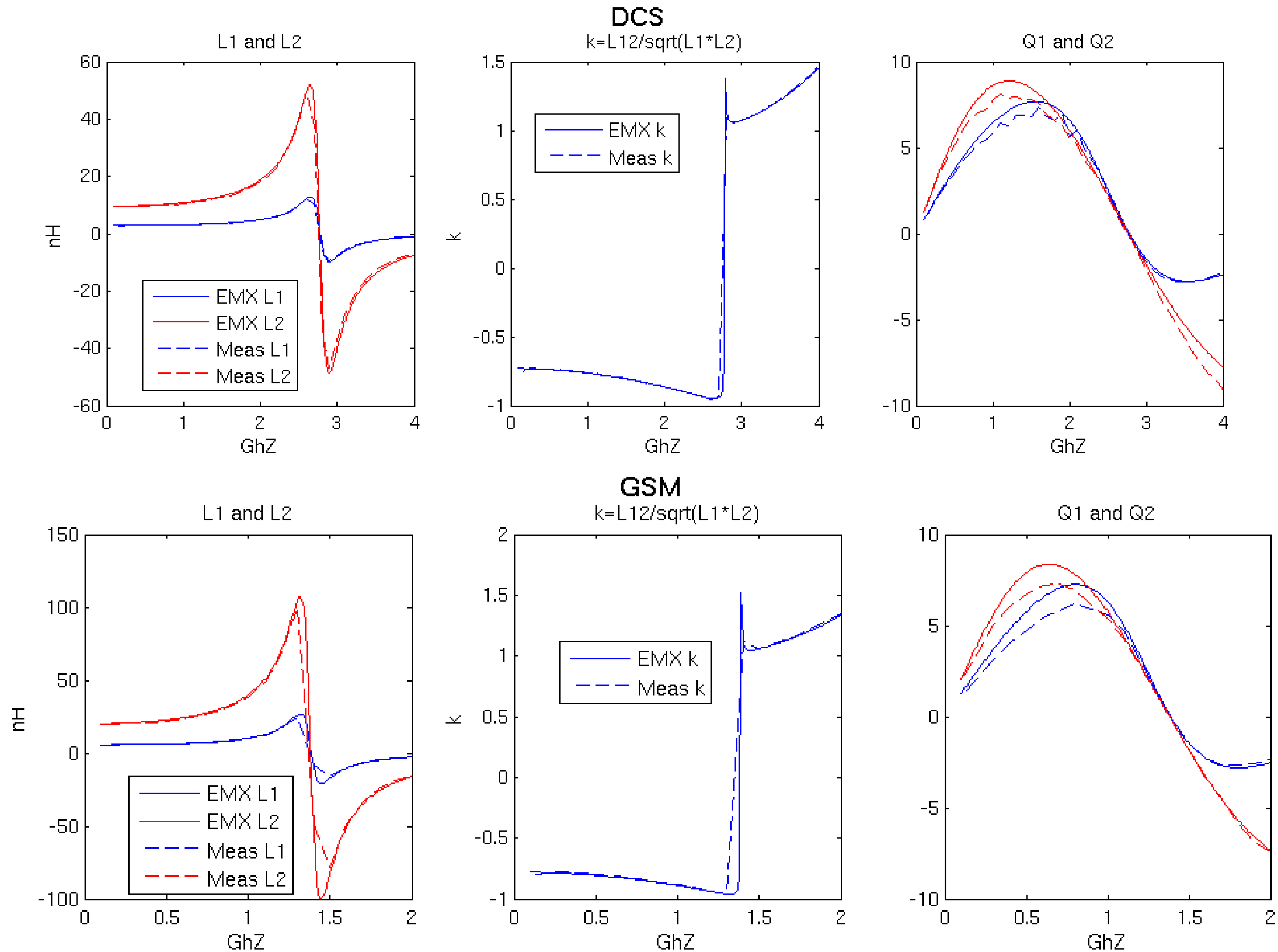
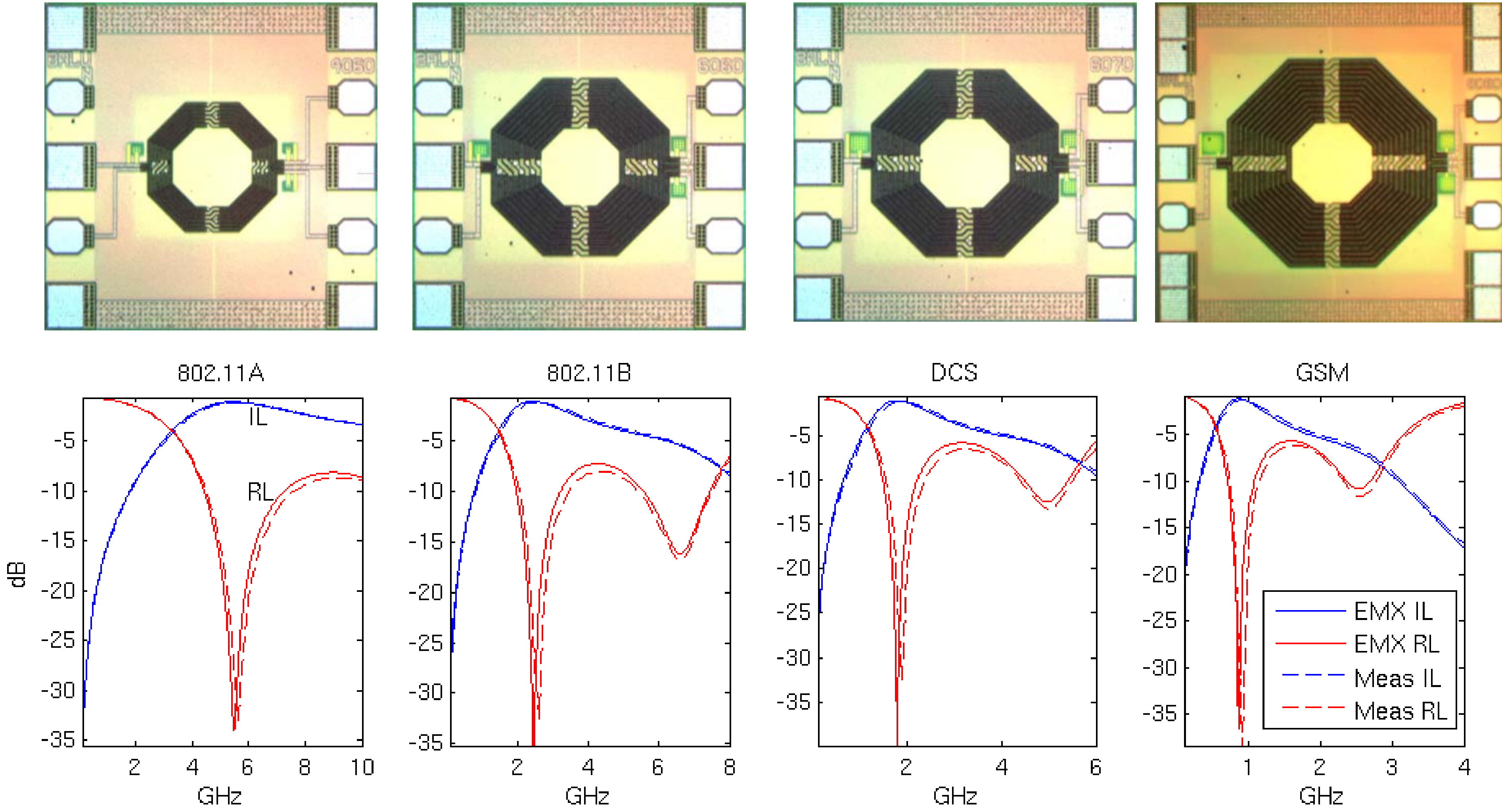
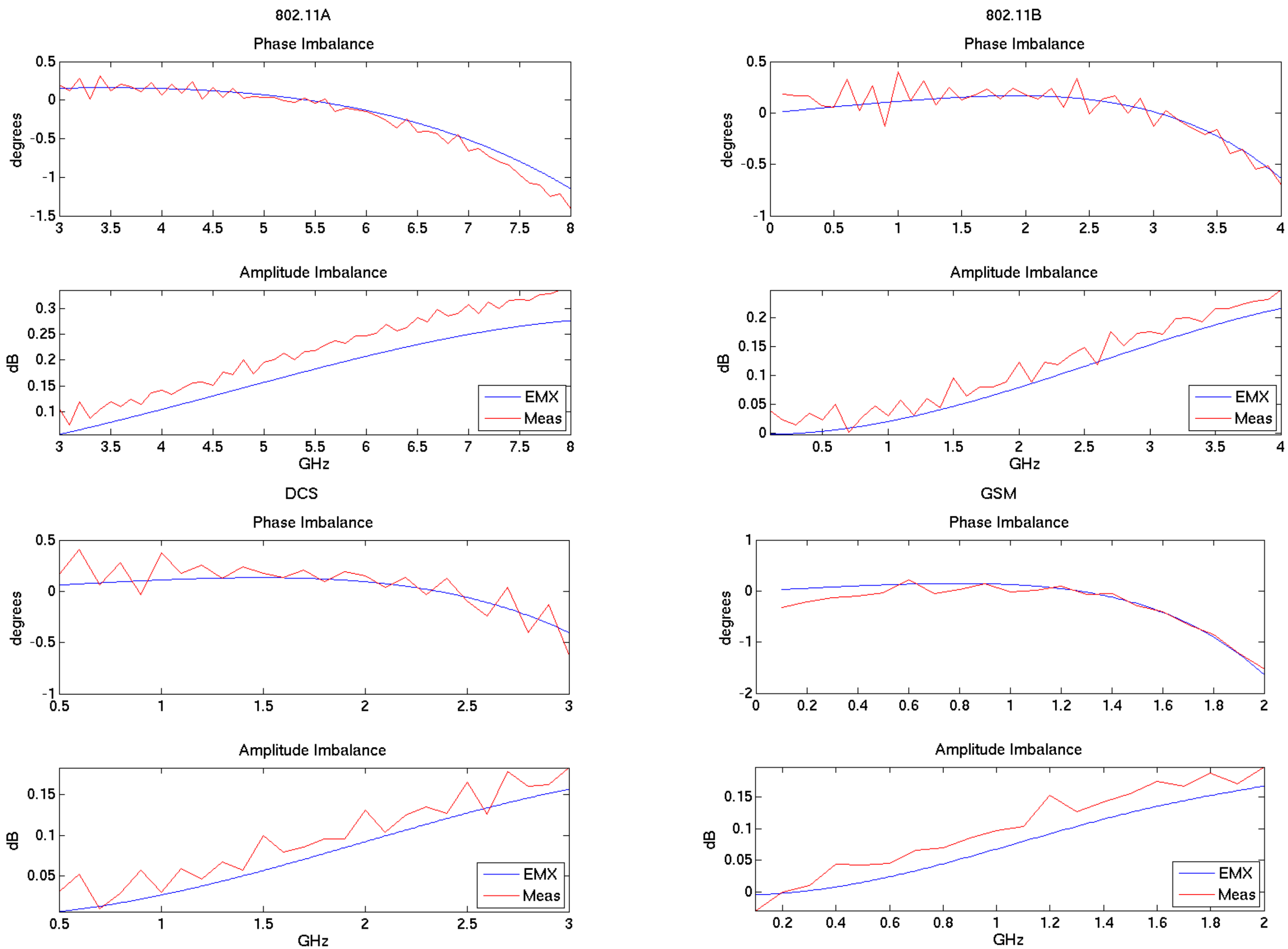


Balun silicon verification (Insertion Loss)



Phase and Amplitude imbalance



Balun summary

- The 4 characterized Baluns have excellent characteristics!
  - Insertion loss of less than 1.5dB
  - Return loss of about 16dB
  - Phase imbalance of less than 0.25 degrees
  - Amplitude imbalance of less than 0.25dB

Balun			Insertion Loss		Return Loss		Phase Imb.		Amplitude Imb.	
Balun	Band	Area	EMX	Meas	EMX	Meas	EMX	Meas	EMX	Meas
802.11A	5115-5825MHz	$185 \times 185\mu m^2$	1.15dB	1.28dB	19.98dB	17.60dB	0.05°	0.16°	0.20dB	0.23dB
802.11B	2400-2483MHz	$255 \times 255\mu m^2$	1.08dB	1.21dB	28.30dB	20.24dB	0.14°	0.26°	0.11dB	0.13dB
DCS	1710-1880MHz	$273 \times 273\mu m^2$	1.16dB	1.43dB	20.83dB	16.39dB	0.13°	0.20°	0.08dB	0.12dB
GSM	824-915MHz	$388 \times 388\mu m^2$	1.19dB	1.44dB	20.98dB	17.03dB	0.15°	0.25°	0.06dB	0.10dB

Comparision to off-chip baluns

Work	Area	IL	PI	AI
Our GSM	$388 \times 388\mu m^2$	1.44dB	0.25°	0.1dB
GSM [1]	$2 \times 1.2mm^2$	1.3dB	3°	0.5dB
Our 802.11B	$255 \times 255\mu m^2$	1.21dB	0.26°	0.12dB
802.11B [2]	$2 \times 1.2mm^2$	0.8dB	7°	0.7dB
802.11B [3]	$3.2 \times 1.6mm^2$	1.02dB	1.23°	0.43dB

[1] A design of the Ceramic Chip Balun using Multilayer Configuration,
D.-W.Lew et al., IEEE MTT, Vol 49, 2001
[2] Design of New-Three Line Balun and its implementation using Multilayer Configuration,
B.H. Lee, et al., IEEE MTT, Vol 54, Jun 2006
[3] Chip-type LTCC-MLC Baluns using the stepped impedance method
C.-W.Tang, et al., IEEE MTT, Vol 49, Dec 2001

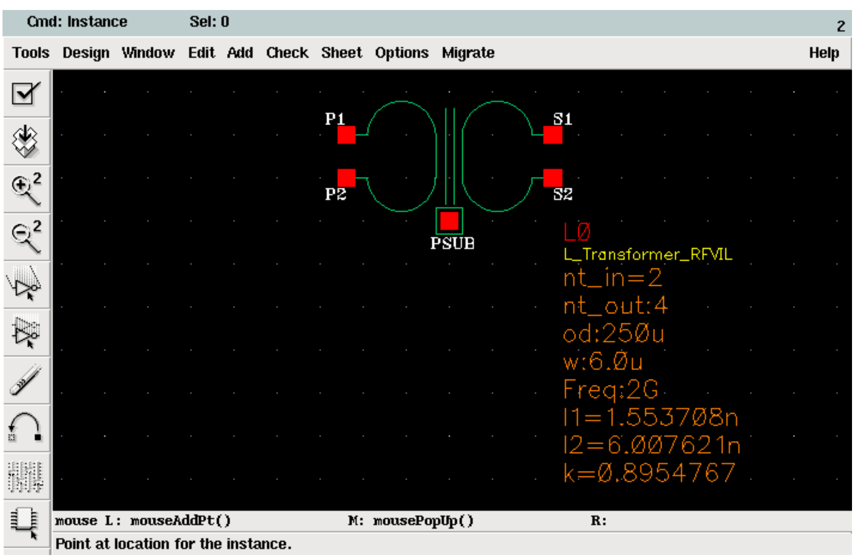
Conclusions

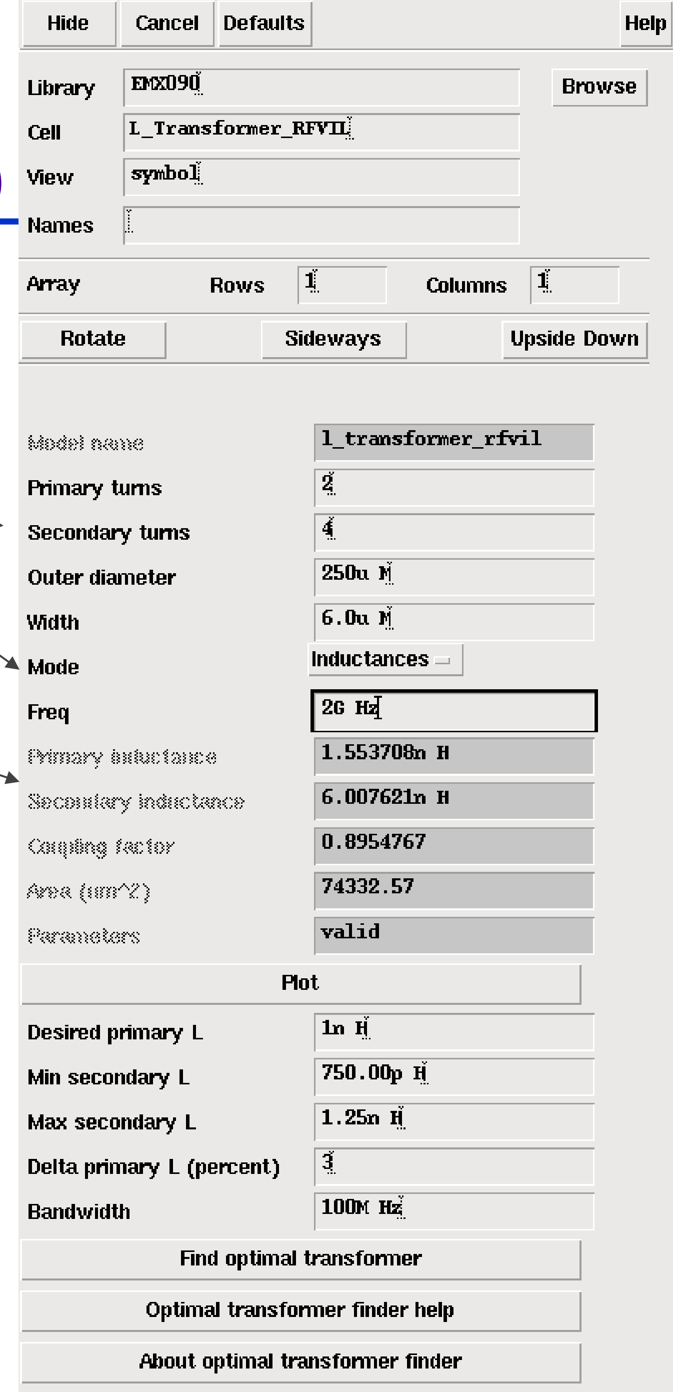
- We described a method for synthesizing optimal on-chip baluns
- The technique involves creating a scalable transformer model from EM simulations.
- This is followed by a fast exhaustive search through design space to find a set of tuning capacitors. The search includes designer-specified constraints on area, bandwidth, insertion loss, return loss etc.
- The method was used to design 4 baluns for common wireless applications. The baluns were fabricated and measured on a 90nm UMC CMOS process
- They were found to operate as predicted and have excellent characteristics. They were found to be equal or better than off-chip baluns while requiring significantly less area

Extra Slides

Inductance Mode (Forward)

1. Select mode
2. Type in Geometric Parameters
3. Obtain Electrical Parameters



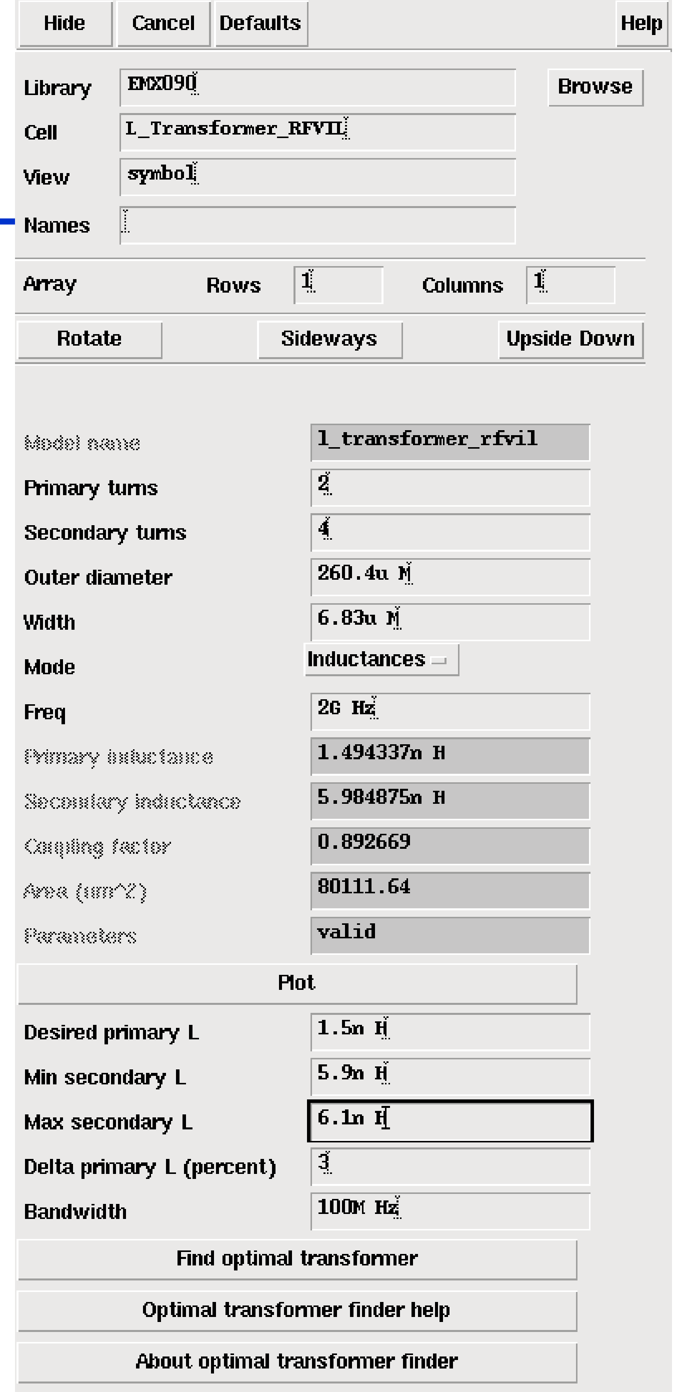


Inductance Mode (design)

4) Give Electrical Parameters

- Give L1 inductance
- Give a range for L2

5) Obtain Geometric Parameters of an optimal transformer



Inductance Mode (plot)