Synthesis of Optimal On-Chip Baluns

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ABSTRACT

We describe a method for synthesizing on-chip baluns. The method involves creating a scalable transformer model from electromagnetic (EM) simulations. Using this model, a quick search through the design space produces an optimal balun. The search may include constraints on insertion loss, return loss, area, etc. We used this method to design baluns for common wireless applications. The baluns were fabricated in a 90nm RF CMOS process and measured. They were found to have good performance with insertion loss less than 1.5dB, return loss of about 16dB, phase imbalance of 0.25° and amplitude imbalance of 0.25dB. These characteristics are equal to or better than those of off-chip baluns while requiring significantly less area.

1. INTRODUCTION

Integrated wireless transceivers frequently use a differential circuit architecture. Since board-level RF connections are commonly single-ended microstrip configurations, and antennas are single-ended as well, many wireless systems require one or two baluns in the front-end. These are usually implemented as discrete components made with multi-layer ceramic or laminate technologies. Commercially available discrete baluns have about 1-1.5dB of insertion loss, up to 1dB of amplitude imbalance and up to 10 degrees of phase imbalance.

The feasibility of implementing transformers on ICs has long been recognized [7]. Practical IC transformers have only modest inductance values (typically several nH) and coupling constant k between 0.6 and 0.9. However, the parasitic leakage inductances in such devices can be combined with resonating capacitors to obtain good transformer characteristics within the frequency band of interest. Although on-chip transformers have been used for internal coupling, their use as baluns has only been reported recently [1, 4, 8, 10, 11].

Since baluns generally occupy a position between the antenna and the receiver input or transmitter output, their losses directly impact noise figure and power efficiency. However, the use of thick metals and low-loss substrates have reduced RF losses sufficiently to make on-chip baluns practical. In this paper we demonstrate that on-chip baluns can be designed to have insertion loss comparable to off-chip LTCC or ceramic baluns. Further, because on-chip baluns are significantly smaller than off-chip baluns, the lower inter-winding capacitance results in significantly better phase and amplitude imbalance. In addition, on-chip baluns allow for greater levels of integration and potentially lower cost.

This paper presents a systematic three-step method for the design of optimal baluns. We start with a transformer layout generator whose inputs are turns ratio, number of turns, trace width and coil diameter. In the first step, we use an EM simulator to characterize the range of possible transformer layouts. In the second step, we use optimization to create an accurate scalable model parameterized by these same inputs. In the third step, we use a higher-level optimizer to choose an optimal transformer layout together with tuning capacitors. Typically, we minimize area given constraints on insertion loss, return loss, etc.

The baluns will be *optimal* within the design space covered by the transformer layout generator and the physical limitations of the process technology. This is not to say that these baluns are optimal over all possible transformer layout styles or different technologies.

Using this technique, we designed four baluns for common wireless applications. The baluns consisted of a transformer and three tuning capacitors. These were baluns with single-ended input impedance Rse of 50Ω and differential output impedance Rdiff of 200Ω (see Figure 1). The baluns were fabricated in a 90nm, 9-level metal IC process, and then measured. The a-priori predicted performance matched almost perfectly with measurement.

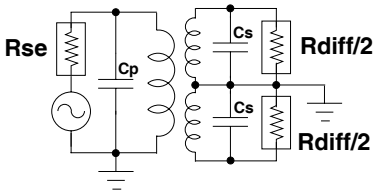

Figure 1: Balun schematic

2. OPTIMAL BALUN SYNTHESIS

The starting point for our balun synthesis method is an automatic layout generator for transformers. The layout of one of our 1:2 transformer is shown in Figure 2. This layout also shows the tuning MIM capacitors used. The shaded routing is the primary winding and the unshaded routing is the secondary. The transformer layout is parameterized by turns ratio, number of turns, width and diameter.

2.1 Electromagnetic simulation using EMX

We generated transformer layouts covering a wide range of geometric parameters: width 4-10μm, 2-5 turns, turns ratio of 1:1 through 1:4, diameter 50-400μm. This resulted in about 1000 transformer layouts. We simulated the layouts with the EMX simulator [2, 3].

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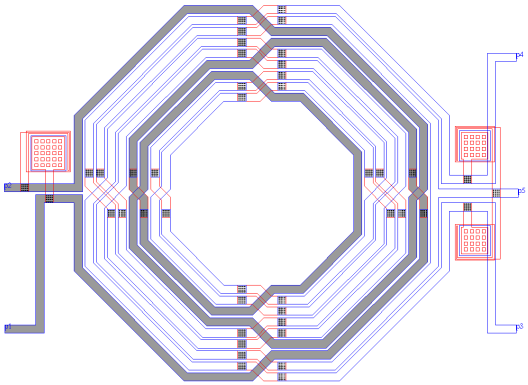

Figure 2: 1:2 Balun layout with MIM capacitors

EMX is a 3D full-wave electromagnetic simulator. It is based on an integral equation formulation of Maxwell's equations. It uses a volume mesh of the conductors and a Green's function to handle layered dielectrics and substrates. It correctly accounts for sidewall capacitance, via resistance and inductance, and current crowding effects. EMX incorporates special features that allow direct simulation of fabrication-ready layout with no hand editing.

EMX uses advanced numeric algorithms for matrix representation and solution. In addition, it exploits geometric regularity and caching techniques to significantly decrease the simulation time and memory. A typical layout as shown in Figure 2 takes a few minutes to simulate. Because of this speed it was possible to simulate the entire design space of 1000 transformers in less than one day using 4 CPUs.

2.2 Building a scalable transformer model

The topology for the scalable model was derived from physical intuition and is shown in Figure 3. The schematic shows a center-tapped pair of coils. Each coil includes additional resistors and inductors for modeling skin-effect. A combination of resistors and capacitors is used to model the substrate.

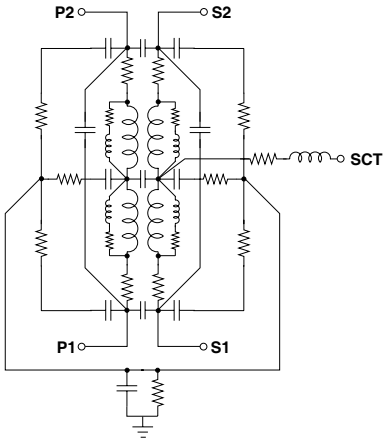

Figure 3: Scalable model schematic

Each element in the model has a value that is a non-linear function of the geometric parameters. The specific forms of these functions are chosen based on physical intuition. For example, the main series resistance in each coil is proportional to the diameter and inversely proportional to the width. The fitting coefficients within the functions are determined by a non-linear least squares optimizer. The objective function for the optimization includes the S-parameters from the simulation, as well as some derived quantities that are correlated with important design metrics such as insertion loss. A playback was done for each set of S-parameters and the model was verified to match within a few percent for derived quantities like inductance, k, Q, etc. For example, the histogram of Figure 4 shows the percentage error in primary inductance L1, secondary inductance L2, and k across the design space. The optimizer took a few hours to build the scalable model.

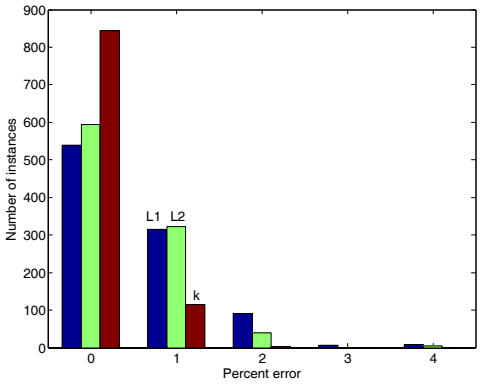

Figure 4: Comparison of model to simulations

2.3 Balun synthesis through optimization

Given the scalable model of the transformer, simulation of the performance of any particular balun (including the tuning capacitors) takes only a fraction of a second. This means that an exhaustive examination of the entire design space can be done in under a minute. Constraints may be placed on any combination of area, insertion loss, return loss (matching), phase imbalance or amplitude imbalance. The entire bandwidth of interest can be checked, and the desired input and output impedances can also be specified during the search. Note that there is no restriction to any particular common set of impedances; they may even be complex numbers if desired. The optimized match can compensate for arbitrary chip loading and for wire-bond and package inductance.

While the EM simulation and the construction of the scalable model is somewhat time-consuming, the actual synthesis of any given balun is very quick. Typically, a foundry would provide the layout generator and the scalable model for a particular process. The end user only has to run the final quick optimization to design a balun for a particular application.

3. MEASUREMENT AND VERIFICATION

The method of the previous section was used to design four baluns for common applications: 802.11A, 802.11B, DCS and GSM. A standard single-ended impedance of 50Ω and a differential output impedance of 200Ω were chosen for demonstration. The baluns were fabricated in a 90nm, 9-level IC process. 3μm copper with sheet resistance 6mΩ/sq was used for the coil, and thinner metals were stacked to form the underpasses. The substrate resistivity was about 20Ω-cm. Tuning MIM capacitors of about 2fF/μm^2 were used. In all the layouts, coil area dominated capacitor area.

For the purposes of detailed verification, two sets of layouts were fabricated. The first set had the four transformers

with center-tap floating in a four port pad frame. The second set was the baluns, i.e., the same transformers along with the tuning capacitors (and the center tap grounded). Chip photos of one transformer and the corresponding balun are shown in Figure 5. The on-wafer four-port S-parameters were measured with an Agilent PLTS 50GHz characterization system which includes the E8364B network analyzer and the N4421B test set. Calibration was done using the four-port Line-Reflect-Match (LRM) procedure with Cascade Microtech Infinity GSGSG probes and an impedance standard substrate. For the purposes of verification, all devices were considered to contain the leads up to the edge of the pad frame. This allowed us to use only an open de-embedding and still have minimal de-embedding artifacts.

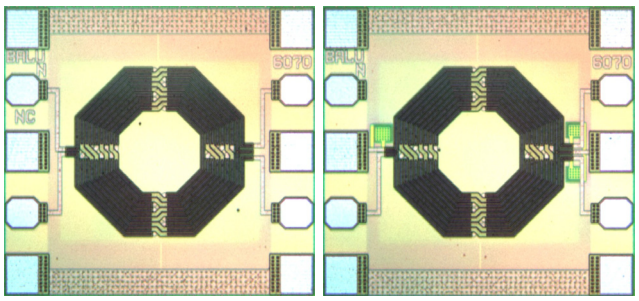

Figure 5: Transformer and balun in padframe

3.1 Transformer measurements

Figure 6 shows the comparison of measurement to the direct EM simulation of the DCS transformer. Simulation was done on the transformer, including the leads up to the pads, as shown in Figure 2. Nominal process parameters were used in the simulation. The agreement is excellent and inductance and k value are within a few percent of measurements across the entire frequency band.

The results were equally good for the other three transformers and are summarized in Table 1, showing the inductance and coupling values at 1GHz.

Balun	L1(nH)		L2(nH)		k	
	EMX	Meas	EMX	Meas	EMX	Meas
802.11A	1.26	1.25	3.84	3.83	0.63	0.64
802.11B	2.46	2.42	8.33	8.17	0.72	0.72
DCS	2.86	2.78	9.79	9.51	0.74	0.74
GSM	6.34	6.11	22.8	21.9	0.81	0.80

Table 1: Transformer characteristics at 1GHz

3.2 Balun measurements

Figure 7 shows the comparison of measurement to the direct EM simulation of the four baluns. The simulations were done on the baluns, including the MIM capacitors and the leads up to the pads, as shown in Figure 2. The agreement between measurement and EMX simulation for all the baluns is very good; the broadband characteristics of the insertion and return loss closely match the measured data.

The results are summarized in Table 2. The first two columns show the balun and the associated frequency band. The columns for the insertion loss, phase imbalance and amplitude imbalance show the maximum values within the frequency band. The return loss columns show the minimum values over the band. For the insertion loss, the results predicted by the a-priori simulation were between 0.13dB and 0.27dB of measurement. The agreement with simulation was also excellent for the other metrics (see Figure 8 for example). The difference between simulation and measurement is mainly due to a shift in the tuning capacitor values away from nominal.

In summary, the measured results for the four baluns show excellent characteristics: insertion loss of less than 1.44dB; return loss of more than 16dB; phase imbalance of less than 0.25°; and amplitude imbalance of less than 0.23dB. For reference, characteristics of some comparable off-chip baluns are given in Table 3.

Work	Area	IL	PI	AI
Our GSM	$388 \times 388\mu m^2$	1.44dB	0.25°	0.1dB
GSM [6]	$2 \times 1.2mm^2$	1.3dB	3°	0.5dB
Our 802.11B	$255 \times 255\mu m^2$	1.21dB	0.26°	0.12dB
802.11B [5]	$2 \times 1.2mm^2$	0.8dB	7°	0.7dB
802.11B [9]	$3.2 \times 1.6mm^2$	1.02dB	1.23°	0.43dB

Table 3: Comparison to off-chip baluns

4. CONCLUSION

We described a method for synthesizing optimal baluns. The method involves creating an accurate scalable transformer model from EM simulations, followed by a fast exhaustive search of the complete design space. The result of the search is a specific transformer layout and a set of tuning capacitor values. The search includes designer-specified constraints on area, bandwidth, insertion loss, return loss, etc. The method was used to design four baluns for common wireless applications. The baluns were fabricated in a 90nm RF CMOS process, and measured; they were found to perform as predicted. The baluns have excellent characteristics, with insertion and return losses equal to those of off-chip baluns, and with better phase and amplitude imbalances. These baluns also have much smaller area than the off-chip baluns.

5. REFERENCES

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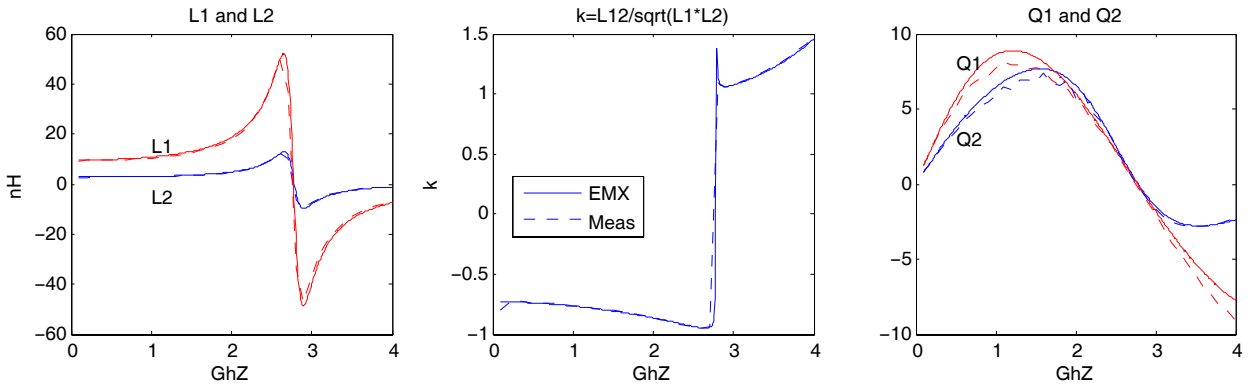

Figure 6: Inductance, k, and Q of the DCS transformer: EMX simulation vs measurement

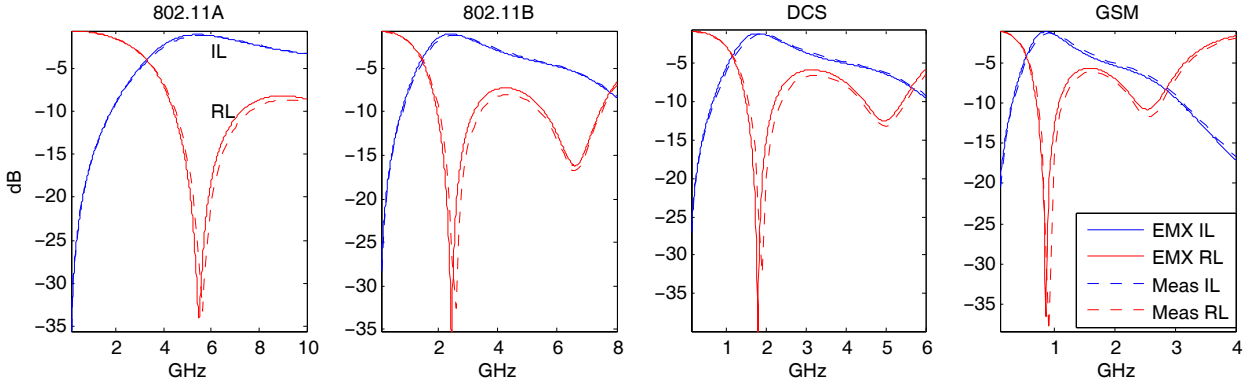

Figure 7: Insertion loss (IL) and return loss (RL) of baluns: EMX simulation vs measurement

Balun			Insertion Loss		Return Loss		Phase Imb.		Amplitude Imb.	
Balun	Band	Area	EMX	Meas	EMX	Meas	EMX	Meas	EMX	Meas
802.11A	5115-5825MHz	$185 \times 185\mu m^2$	1.15dB	1.28dB	19.98dB	17.60dB	0.05°	0.16°	0.20dB	0.23dB
802.11B	2400-2483MHz	$255 \times 255\mu m^2$	1.08dB	1.21dB	28.30dB	20.24dB	0.14°	0.26°	0.11dB	0.13dB
DCS	1710-1880MHz	$273 \times 273\mu m^2$	1.16dB	1.43dB	20.83dB	16.39dB	0.13°	0.20°	0.08dB	0.12dB
GSM	824-915MHz	$388 \times 388\mu m^2$	1.19dB	1.44dB	20.98dB	17.03dB	0.15°	0.25°	0.06dB	0.10dB

Table 2: Balun performance: EMX simulation vs measurement

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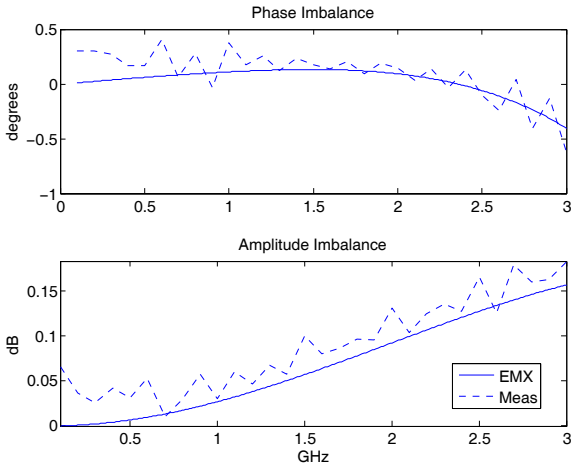

Figure 8: Amplitude and phase imbalance of DCS Balun: EMX simulation vs measurement