

Including Pattern-Dependent Effects in Electromagnetic Simulations of On-Chip Passive Components

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Abstract—In advanced IC processes, the physical properties of wires (width, thickness, and resistance) vary depending on the surrounding wiring. We modified the EMX electromagnetic simulator to allow width- and spacing-dependent properties to be given in the process description. EMX automatically modifies the drawn layout to mimic the fabrication process. We validate our approach by comparing to measurements and showing that this significantly improves simulation accuracy for inductors and interdigitated capacitors.

I. INTRODUCTION

In advanced IC nodes, the physical width, thickness, and resistance of a wire generally depends on the surrounding wiring. Sometimes the variations are very significant. Fabricated widths may vary by up to 50% from the nominal (drawn) width, and sheet resistance can change by a factor of two. Such variations are called *pattern-dependent* effects. Because these effects can be so large, it is important to account for them in simulation and modeling.

These effects are especially critical in interdigitated capacitors (also called finger capacitors or MoM capacitors). In modern processes that have many metal layers, MoM capacitors are generally preferred over thin-film capacitors because they offer higher capacitor density and because they do not require extra processing steps. Since these capacitors are very regular, any error in computing the sidewall capacitance for a single finger causes an almost identical error in the overall model of the capacitor.

Inductors built using multiple metal layers (stacked inductors) are also very sensitive to pattern-dependent effects. These inductors are designed to take up minimal area by winding a spiral up through several layers. The Q of a stacked inductor depends heavily on the sheet resistance.

Some foundries provide detailed information about pattern dependencies. This information is usually in the form of tabulated data, with the tables indexed by wire width and spacing to adjacent wires. An example is the interoperable R(L)C extraction technology file format iRCX [1], [2]. This file format is now used for both static RLC extraction and high frequency EM simulations. Many layout parasitic extraction tools make use of local width and spacing information during capacitance and resistance extraction. However, these tools mostly work by analyzing 2-dimensional cross sections

through the wiring. While they provide reasonable accuracy for analyzing parasitic effects, they are not designed for making high-accuracy, frequency-dependent models of passive components.

Electromagnetic (EM) simulation tools can give higher accuracy, but most do not offer methods for automatically taking pattern dependencies into account. This makes using such tools for component modeling difficult in practice. Either inaccuracy must be accepted, or the input layout and process information must be altered to try to mimic the fabricated layout. The latter can be difficult even in simple cases, and may not be possible in other situations.

In this paper, we describe a method for automatically modeling pattern-dependent effects within the EMX [3], [4] simulator. EMX's process file format allows the specification of width and spacing dependencies. Internally, the tool automatically modifies the input (drawn) layout order in order to accurately model the fabricated structure. This paper describes the techniques used by the simulator for constructing the internal modified layout. We show that EMX can model MoM capacitors and stacked inductors whose behavior is sensitive to pattern dependencies. We also verify the accuracy of EMX used in conjunction with an iRCX technology file by comparing to measurements.

II. INCORPORATING PATTERN-DEPENDENCE IN EMX

EMX is a 3D full-wave electromagnetic simulator. It is based on an integral equation formulation of Maxwell's equations, and it uses advanced numeric algorithms to significantly decrease the simulation time and memory. EMX uses a volume mesh of the conductors and a Green's function to handle layered dielectrics and substrates. It correctly accounts for sidewall capacitance, via resistance and inductance, and current crowding effects. It incorporates special features that allow direct simulation of fabrication-ready layout with no hand editing.

Modifying EMX to handle pattern-dependent effects required:

- devising appropriate definitions of the local width, spacing, etc.; and
- developing efficient algorithms for computing these quantities, and for manipulating the input (drawn) geometry

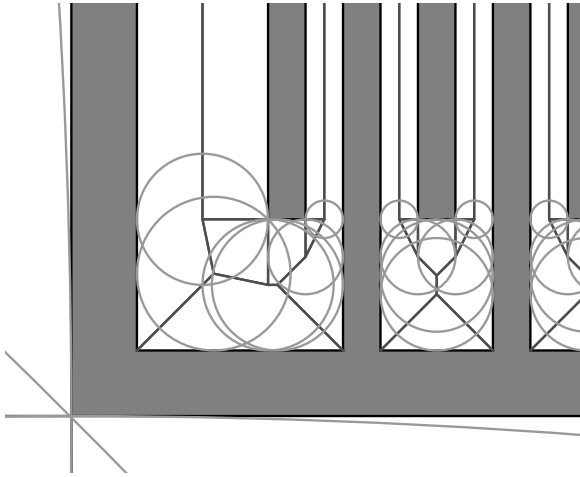


Fig. 1. Exterior Voronoi diagram of some wiring

as a function of them.

A. Computing width and spacing

For simple repetitive layout (e.g., multiple parallel wires) width and spacing have intuitive meanings. However, a simulator must handle more complicated situations involving non-uniform layout. We want definitions that match the intuitive meanings in regular regions and that lend themselves to efficient computation. For width and spacing, a natural geometric data structure for representing local distances between objects is the *Voronoi diagram* [5].

In the case of IC layout, the objects of interest are line segments representing the edges of wires, and points where segments join. Each segment and point has a region around it that is closer to that object than to any other object. Following this idea, the entire plane is partitioned into non-overlapping regions, and this partitioning is the Voronoi diagram of the segments and points. Note that part of the Voronoi diagram lies within the wiring, and the rest lies outside. These two parts are called the interior and exterior Voronoi diagrams.

A bit of MoM capacitor layout and the associated exterior Voronoi diagram is shown in figure 1. The shaded areas are the wires. Between the wires, there are some segments which represent the boundaries of the Voronoi regions.¹ Also shown are some circles. These are *maximal inscribed circles*. Each circle just touches three objects, and the circles cannot be made any bigger while touching those objects.

For most segments, we define the local spacing to be the diameter of the appropriate maximal inscribed circle that touches the segment and the nearest other object(s). However, we include an exception for segments at the edge of the layout. For such segments, the maximal inscribed “circle” extends to infinity. While this is a valid value for the spacing, it leads to a spacing function that can change very quickly as a function of position. For such cases, we take the value of the spacing from the neighboring segments in the layout.

¹Technically, some of the boundaries are parts of parabolas, but computationally it is easier to approximate these parts by segments.

$w \setminus s$	0.1000	0.1300	0.1500	0.2000	...
0.1000	0.1025	0.1125	0.1220	0.1470	...
0.1300	0.1265	0.1285	0.1340	0.1525	...
0.1500	0.1459	0.1459	0.1459	0.1599	...
0.2000	0.1783	0.1783	0.1783	0.1783	...
...

Fig. 2. Physical width (microns) as a function of drawn width and spacing

The local width is calculated in the same way as the local spacing, except we use the interior Voronoi diagram instead of the exterior one. For width calculations, it is not possible to have a maximal inscribed circle of infinite diameter.

Local width and spacing are calculated at key points throughout the layout during the Voronoi diagram construction. Afterwards, the values can be quickly interpolated at any desired location.

B. Physical width variation

Probably the most significant fabrication effect is that physical line width differs from the drawn width by a *bias* amount which depends on the local width and spacing in the layout. The bias is obtained from a table provided by the foundry. Figure 2 shows an example of a table giving the physical width of a metal wire as a function of the drawn width and spacing. For example, a $0.1 \mu\text{m}$ drawn wire at a spacing of $0.2 \mu\text{m}$ will physically expand to be $0.147 \mu\text{m}$ wide. That represents an increase of almost 50% from the drawn width.

By interpolating in such a table, we get a continuous function for the bias as a function of drawn width and spacing. Also, the local width and spacing vary continuously with the location in the layout. For practical purposes, we restrict the allowed variation by dividing the edges in the layout into segments of at most a user-specified length. We average the bias along each segment to get an overall bias for the segment. Then, for each point between segments, we displace each point based on the bias and orientation of the adjacent two segments. An example of a layout before and after the bias operation is shown in figure 3. Note that the biased geometry is not rectilinear when the width and spacing are not uniform.

C. Sheet resistance variation

Another significant effect is sheet resistance variation. This is somewhat easier to handle than biasing. Once we have calculated the local width and spacing and the biased geometry, we simply proceed with mesh generation as normal. At each point in the mesh, we can calculate the sheet resistance as a function of width and spacing. So for each shape in the mesh, we just average the calculated sheet resistance over the area of the shape. An example of a resistance variation table is shown in figure 4. Note that the sheet resistance varies by almost a factor of two as a function of width and spacing. Figure 5 shows the variation in sheet resistance for a MoM capacitor.

Thickness also varies as a function of width and spacing, though this effect is generally smaller (about 10%). It may be

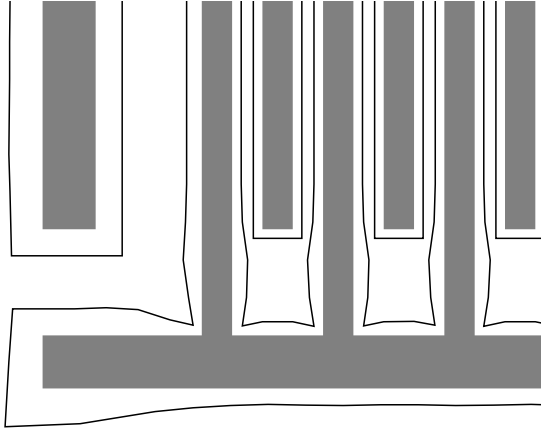


Fig. 3. Wires before (gray) and after (outline) bias

$w \backslash s$	0.1000	0.1300	0.1500	0.2000	...
0.1000	0.1399	0.1220	0.1084	0.0839	...
0.1300	0.1355	0.1316	0.1235	0.1034	...
0.1500	0.1285	0.1275	0.1266	0.1116	...
0.2000	0.1315	0.1305	0.1295	0.1286	...
...

Fig. 4. Sheet resistance (ohms/square) as a function of drawn width and spacing

handled after mesh generation in essentially the same way as sheet resistance.

III. EXAMPLES AND COMPARISON TO MEASUREMENT

In this section, we show comparisons between simulations and measurements for components fabricated in a 65nm 9 metal layer stack. On-wafer two-port S-parameters were measured with an Agilent 8510 network analyzer system.

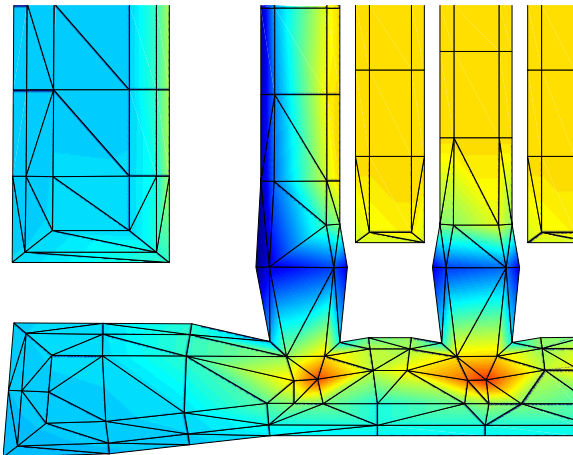


Fig. 5. Variation of sheet resistance in the mesh

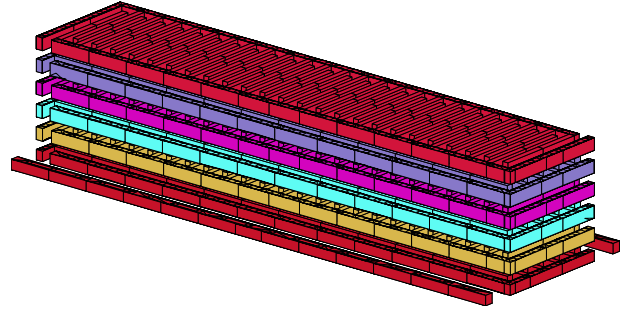


Fig. 6. 3D mesh for MoM capacitor

cell w, s μm	meas pF	iRCX		no iRCX	
		pF	%err	pF	%err
MOM06 0.1, 0.1	0.611	0.617	0.9	0.614	0.5
MOM67 0.16, 0.16	0.293	0.295	0.7	0.300	2.4
MOM27 0.1, 0.16	0.061	0.061	0.3	0.053	-13.1
MOM36 0.1, 0.16	0.682	0.680	-0.2	0.591	-13.3

Fig. 7. Measured and simulated MoM capacitor values at various widths and spacings of fingers

A. MoM capacitors

For the purposes of detailed verification, we used EMX to simulate a set of MoM capacitors. The capacitors varied in the number of metals used, the widths of the metal fingers, and the spacings between fingers. For this 65nm technology the minimum width and minimum spacing are both $0.1 \mu\text{m}$. Figure 6 shows the 3D mesh of one of the capacitors.

We did two simulations: once with the wire properties fixed at their minimum-width, minimum-spacing values (no iRCX), and once with the full iRCX information that allows EMX to mimic the fabricated layout. Figure 7 shows the measured and simulated (low frequency) capacitance values for these MoM capacitors. For capacitors with minimum width and minimum spacing, both simulations provided excellent agreement with measurements. However, for MOM36 with width $0.1 \mu\text{m}$ and spacing $0.16 \mu\text{m}$ there is a 0.2% error when the iRCX file is used and a 13% error when it is not. This ties in with the iRCX table in figure 2, which shows that the bias is most significant for wires that have increased width or spacing.

Figures 8 and 9 show the high-frequency characteristics of the capacitors. For MOM06, with minimum width and spacing, both iRCX and non-iRCX simulations agree well with measurements. However, for MOM36 the iRCX simulation has excellent agreement while the and non-iRCX simulations has a large discrepancy in C and Q.

B. A stacked inductor

We used EMX to simulate a stacked inductor (which is sensitive to pattern dependence). This inductor winds from

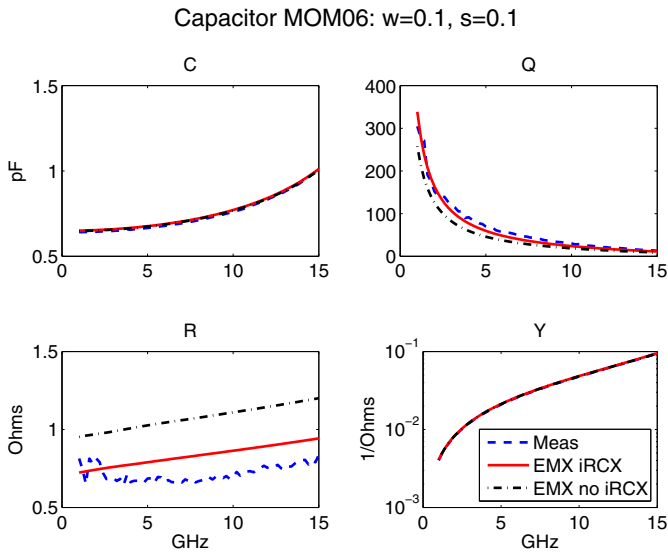


Fig. 8. Comparison of MoM capacitor simulation to measurement for a capacitor using minimum width and spacing

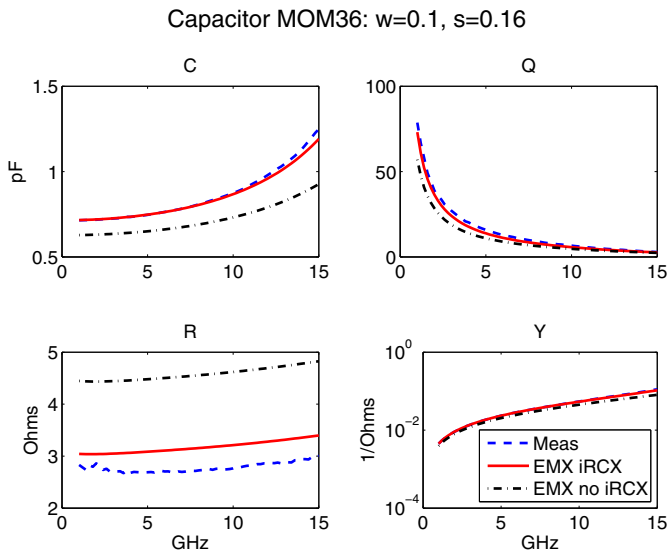


Fig. 9. Comparison of MoM capacitor simulation to measurement for a capacitor using non-minimum width and spacing

metal 5 through metal 9, and includes two thin metals as well as the two thicker ones. The Q of the inductor depends significantly on the resistance in the thin metals, and this resistance varies as a function of metal width and the spacing to nearby wires. Figure 10 shows the EMX mesh for the inductor and the surrounding guard ring. We simulated the inductor with iRCX and without. The iRCX file in figure 4 indicates that the metal sheet resistance is significantly reduced for the wider wires and looser spacings used in the inductor. This is exactly the effect seen in measurement (figure 11).

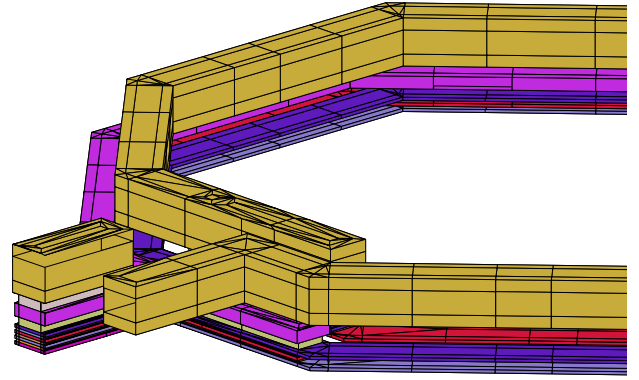


Fig. 10. Section of a 3D mesh for stacked inductor

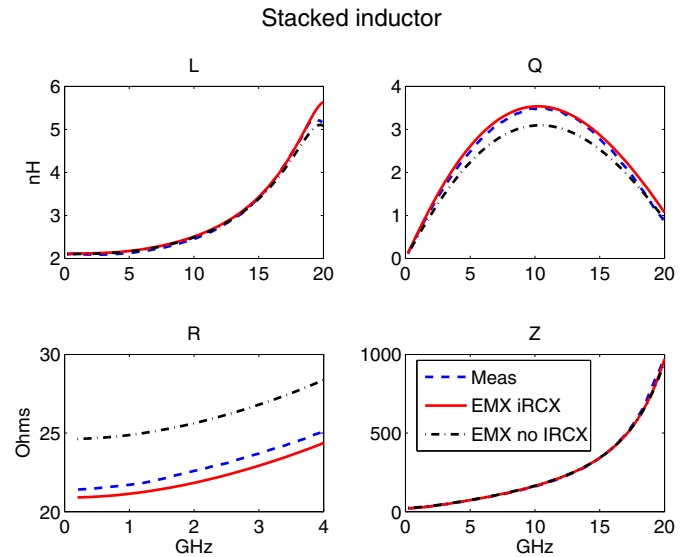


Fig. 11. Comparison of stacked inductor simulation to measurement

IV. CONCLUSION

Pattern-dependent effects are significant in many modern IC processes. We have described how the EMX electromagnetic simulator automatically incorporates width and spacing dependencies to mimic the fabricated layout. A number of MoM capacitors and stacked inductors were built on a 65 nm process. The iRCX technology file format was used by EMX to simulate these structure and found to significantly improve simulation accuracy as demonstrated through comparisons to measurements.

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